



# CIRCUITS INTEGRES

## PORTES LOGIQUES

	FAMILLE LOGIQUE								
	Type	STD	LS	HCT	HC	FAST	AC	ACT	F
<b>ET</b>									
Quatre portes ET à 2 entrées	08								
Trois portes ET à 3 entrées	11								
Deux portes ET à 4 entrées	21								
<b>OU</b>									
Quatre portes OU à 2 entrées	32								
Quatre portes OU exclusifs à 2 entrées	86								
Quatre portes OU exclusifs à 2 entrées, C.O.	136								
<b>ET-NON</b>									
Quatre portes ET-NON à 2 entrées	00								
Quatre portes ET-NON à 2 entrées, C.O.	03								
Trois portes ET-NON à 3 entrées	10								
Deux portes ET-NON à 4 entrées	20								
Deux portes ET-NON à 4 entrées, C.O.	22								
Une porte ET-NON à 8 entrées	30								
4 portes amplificatrices ET-NON à 2 entrées	37								
4 portes amplificatrices ET-NON à 2 entrées, C.O.	38								
<b>OU-NON</b>									
Quatre portes OU-NON à 2 entrées	02								
Trois portes OU-NON à 3 entrées	27								
Deux portes OU-NON à 4 entrées	4002								
<b>INVERSEURS</b>									
Six triggers de Schmitt, inverseurs	14								
4 portes ET-NON trigger de Schmitt à 2 entrées	132								
<b>AMPLIFICATEURS</b>									
Six inverseurs	04								
Six inverseurs, C.O.	05								
Six inverseurs-amplificateurs, C.O., 30 V	06								
Six amplificateurs, C.O., 30 V	07								
Quatre amplificateurs 3 états	125								
Quatre amplificateurs 3 états	126								
Double et quadruple amplif. 3 états	367								
Double et quadruple amplif.-inverseurs 3 états	368								

## AMPLIFICATEURS DE BUS

	FAMILLE LOGIQUE								
	Type	STD	LS	HCT	HC	FAST	AC	ACT	F
Octuple amplificateur de ligne invers., 3 états	240								
Octuple amplificateur de ligne, 3 états	241								
2 quadruples amplificateurs de ligne, 3 états	244								
Octuple amplif. de ligne, bidirectionnel, 3 états	245								
Octuple amplif.-inverseur de ligne, 3 états	540								
Octuple amplificateur de ligne, 3 états	541								
Oct. émetteur-récepteur invers. de bus, 3 états	623								
Oct. émetteur-récepteur invers. de bus, 3 états	640								
Oct. émetteur-récept. r de bus + registre, 3 états	646								
Octuple émetteur-récepteur inverseur de bus avec registre, 3 états.	648								
Six amplif.-inverseurs adaptateurs de niveaux	4049								
Six amplificateurs adaptateurs de niveaux	4050								

## BASCULES

	FAMILLE LOGIQUE								
	Type	STD	LS	HCT	HC	FAST	AC	ACT	F
<b>BASCULES D</b>									
Deux bascules type D, 1R, 1S	74								
Deux fois 2 verrous	75								
Quadruple bascule D 4 bits, 3 états	173								
Sextuple bascule type D	174								
4 bascule type D, sorties complémentaires	175								
Octuple bascule D, 3 états	374								
Octuple bascule D, avec validation	377								
Sextuple bascule D, avec validation	378								
Oct. bascule type D, sorties complém. 3 états	534								
Octuple verrou type D, 3 états	573								
Octuple bascule type D, 3 états	574								
<b>BASCULES JK</b>									
Deux bascules JK, 1K, 1R, 1J	73								
2 bascules JK à déclenchement sur front montant	109								
<b>MULTIVIBRATEURS MONOSTABLES</b>									
2 multivibrateurs monostables redéclenchables	123								
2 multivibr. monostables avec triggers de Schmitt	221								
2 multivibrateurs	4538								

## BASCULES (suite)

	FAMILLE LOGIQUE								
	Type	STD	LS	HCT	HC	FAST	AC	ACT	F
<b>VERROUS</b>									
Un verrou adressable 8 bits, validation et RAZ	259								
Octuple bascule type D, RAZ	273								
Quatre bascules RS	279								
Octuple verrou, 3 états	373								
Quadruple multiplexeur 2 vers 1 avec mémoire	399								
Oct. verrou type D, sorties complém.s 3 états	563								
Octuple bascule type D, sorties complém. 3 états	564								
<b>FONCTIONS ARITHMÉTIQUES</b>									
Comparateur 4 bits	85								
Un additionneur binaire 4 bits	283								
Comparateur 8 bits, sortie complémentée	520								
Comparateur 8 bits, sortie complémentée	521								
Compar. d'égalité 8 bits, validation de la sortie	688								
<b>COMPTEURS</b>									
Une décade de comptage sortie 4 bits	90								
Un compteur-diviseur par 2, 6, 12	92								
Un compteur binaire 4 bits	93								
Un compteur binaire 4 bits, reset asynchrone programmable	161								
Un compteur binaire 4 bits programmable	163								
RAZ synchrone	169								
1 compteur-décompteur binaire 4 bits progrblé	191								
1 compteur-décompteur binaire 4 bits	192								
1 compteur-décompteur BCD 4 bits	193								
1 compteur-décompteur binaire 4 bits	393								
Deux compteurs binaires 4 bits	4020								
Un compteur binaire 14 bits	4040								
Un compteur binaire 12 bits	4060								
Un compteur-diviseur binaire 14 étages avec oscillateur	4060								

## REGISTRES À DÉCALAGE

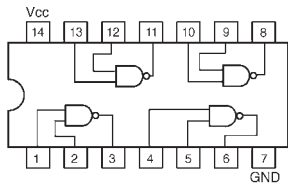
	FAMILLE LOGIQUE								
	Type	STD	LS	HCT	HC	FAST	AC	ACT	F
Un registre à décalage 8 bits, entrées séries sorties parallèles	164								
Un registre à décalage 8 bits entrées parallèles, sortie série	165								
Un registre à décalage 8 bits, entrées séries ou parallèles, RAZ	166								
Un registre à décalage universel 8 bits, 3 états	299								
Un registre à décalage universel 8 bits	323								
Un registre à décalage 8 bits avec registre de sortie, 3 états	595								
Un registre à décalage à 8 étages, sortie parallèle, verrou 3 états	4094								

## DÉCODEURS, MULTIPLEXEURS, DÉMULTIPLEXEURS

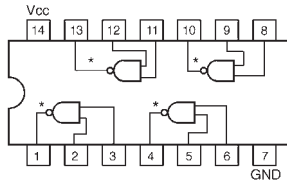
	FAMILLE LOGIQUE								
	Type	STD	LS	HCT	HC	FAST	AC	ACT	F
Décodeur BCD-décimal	42								
Décodeur BCD-7 segments, C.O. (15 V)	47								
1 décodeur-démultiplexeur 3 vers 8 entrées mémorisées	137								
1 décodeur-démultiplexeur 3 vers 8	138								
Deux décodeurs-démultiplexeurs 2 vers 4	139								
1 décodeur BCD-décimal, C.O. (15 V)	145								
1 codeur de priorité 8 vers 3	148								
1 multiplexeur 8 vers 1, sorties complém.	151								
Double multiplexeur 4 vers 1	153								
Double décodeur-démultiplexeur 2 vers 4, C.O.	156								
Quadruple multiplexeur 2 vers 1	157								
Quadruple multiplexeur 2 vers 1 sorties complémentées	158								
Un décodeur-démultiplexeur 3 vers 8 avec adresses mémorisées	237								
Un décodeur-démultiplexeur 3 vers 8	238								
Un multiplexeur 8 vers 1, 3 états	251								
Un double multiplexeur 4 vers 1, 3 états	253								
Un quadruple multiplexeur 2 vers 1, 3 états	257								
Un quadruple multiplexeur 2 vers 1 sortie complémentée, 3 états	258								
Un générateur-contrôleur de parité 9 bits	280								
1 multiplexeur-démultiplex. analogique 8 voies	4051								
Double multiplexeur-démultiplex. analog. 4 voies	4052								
Triple multiplexeur-démultiplex. analog. 2 voies	4053								



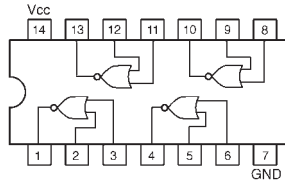
**74 00** 4 portes ET-NON à 2 entrées



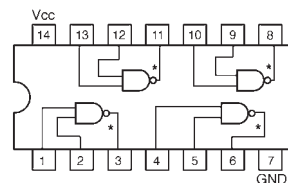
**74 01** 4 portes ET-NON à 2 entrées C.O.



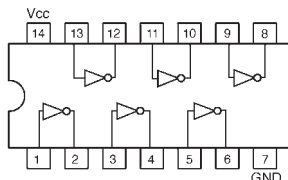
**74 02** 4 portes OU-NON à 2 entrées



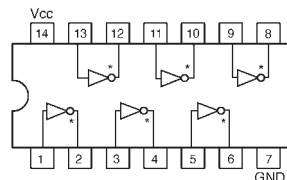
**74 03** 4 portes ET-NON à 2 entrées C.O.



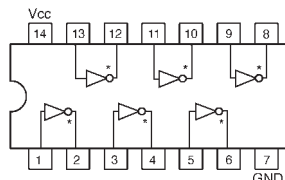
**74 04** 6 inverseurs



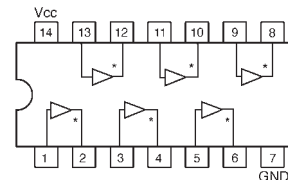
**74 05** 6 inverseurs C.O.



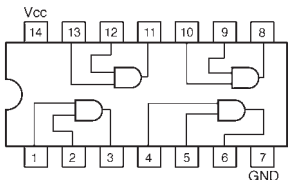
**74 06** 6 inverseurs C.O. 30 V



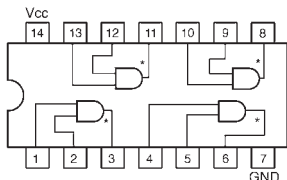
**74 07** 6 amplificateurs C.O. 30 V



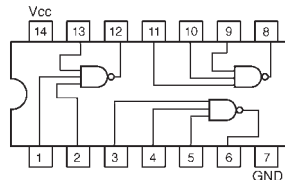
**74 08** 4 portes ET à 2 entrées



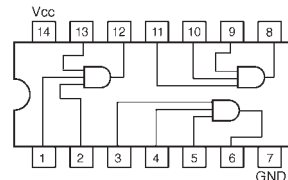
**74 09** 4 portes et à 2 entrées C.O.



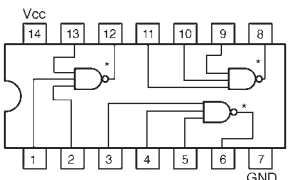
**74 10** 3 portes ET-NON à 3 entrées



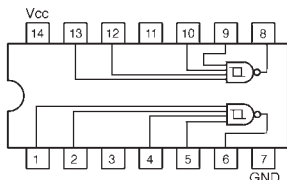
**74 11** 3 portes ET à 3 entrées



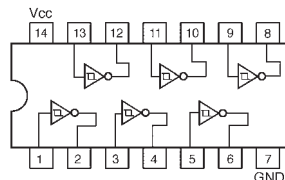
**74 12** 3 portes ET-NON à 3 entrées C.O.



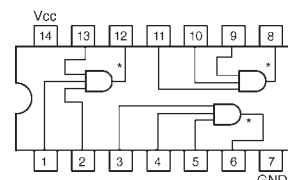
**74 13** 2 portes ET-NON à 4 entrées avec bascule de schmitt



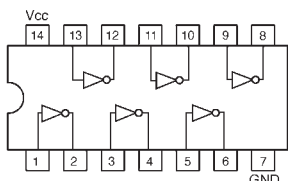
**74 14** 6 inverseurs avec bascule de schmitt



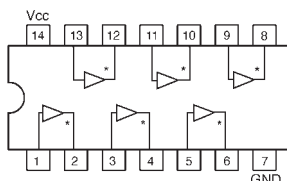
**74 15** 3 portes ET à 3 entrées C.O.



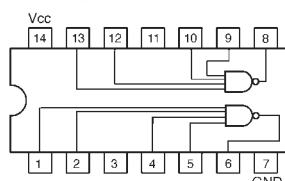
**74 16** 6 inverseurs C.O.



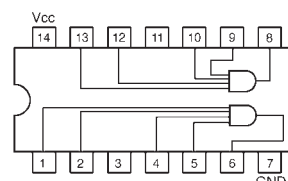
**74 17** 6 amplificateurs C.O. 15 V



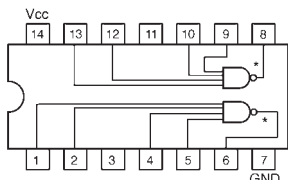
**74 20** 2 portes ET-NON à 4 entrées



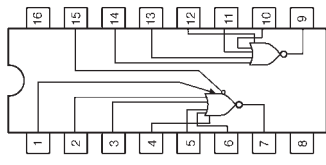
**74 21** 2 portes ET à 4 entrées



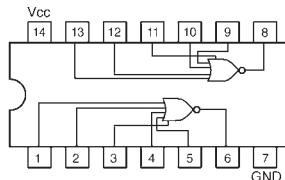
**74 22** 2 portes ET-NON à 4 entrées C.O.



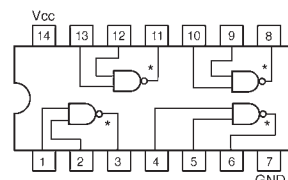
**74 23** 2 portes OU-NON à 4 entrées avec échantillonnage et 1 expansible



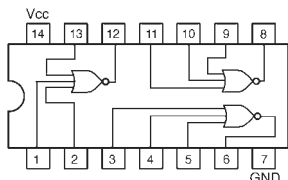
**74 25** 2 portes OU-NON à 4 entrées et échantillonnage



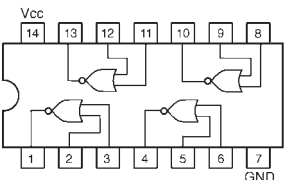
**74 26** 4 portes ET-NON à 2 entrées C.O.



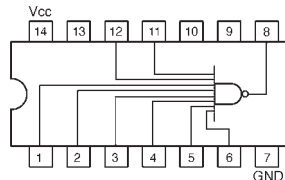
**74 27** 3 portes OU-NON à 3 entrées



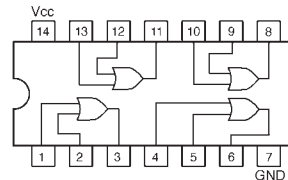
**74 28** 4 portes OU-NON à 2 entrées



**74 30** 1 porte ET-NON à 8 entrées



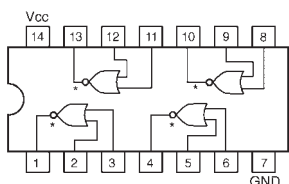
**74 32** 4 portes OU à 2 entrées



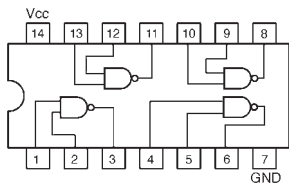


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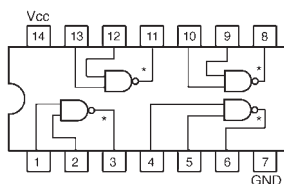
**74 33** 4 portes OU-NON à 2 entrées C.O.



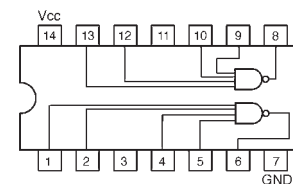
**74 37** 4 portes amplificatrices ET-NON à 2 entrées



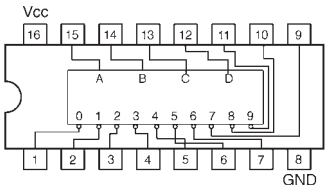
**74 38** 4 portes amplificatrices ET-NON à 2 entrées C.O.



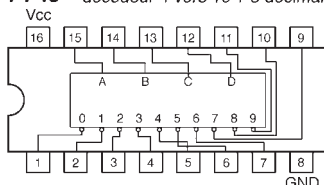
**74 40** 2 portes ET-NON à 4 entrées



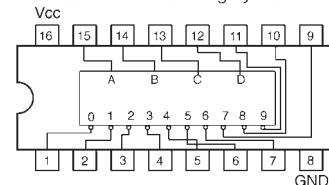
**74 42** décodeur 4 vers 10 BCD décimal



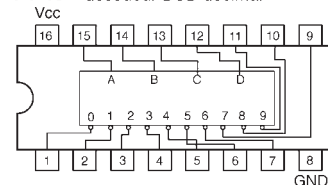
**74 43** décodeur 4 vers 10 + 3 décimal



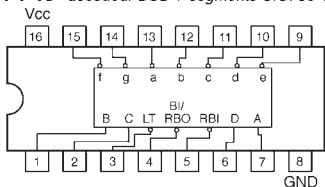
**74 44** décodeur 4 vers 10 gray + 3 décimal



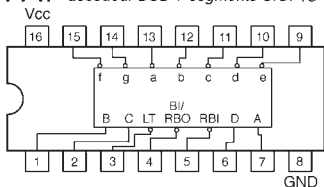
**74 45** décodeur BCD décimal



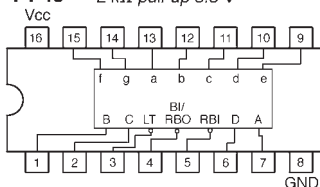
**74 46** décodeur BCD-7 segments C.O. 30 V



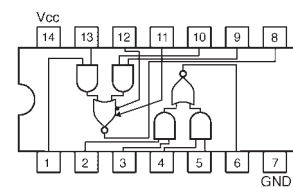
**74 47** décodeur BCD-7 segments C.O. 15 V



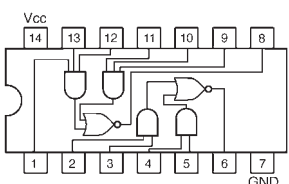
**74 48** décodeur BCD-7 segments 2 kΩ pull-up 5,5 V



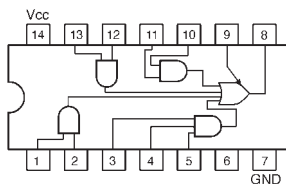
**74 50** 2 portes OU-NON avec 2 ET à 2 entrées dont 1 expansible



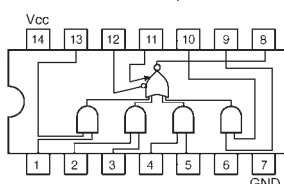
**74 51** 2 portes ET-OU-NON à 2 x 2 entrées



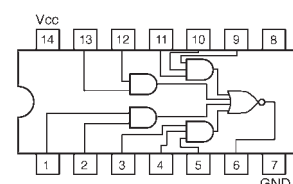
**74 52** Expandable 2 2 2 3 inp. AND OR



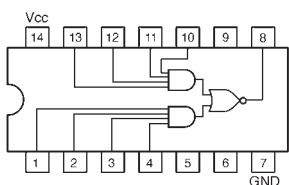
**74 53** 1 porte OU-NON avec 4 ET à 2 entrées expansible



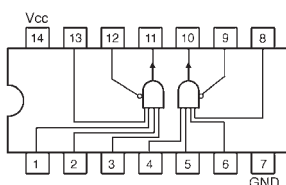
**74 54** 4 wide AND OR INV



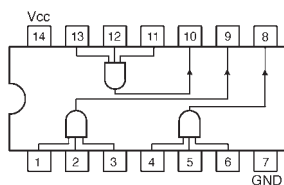
**74 55** 1 porte OU-NON avec 2 ET à 4 entrées



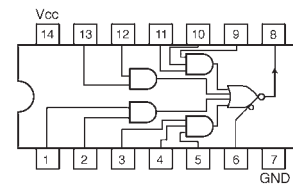
**74 60** 2 extenseurs à 4 entrées



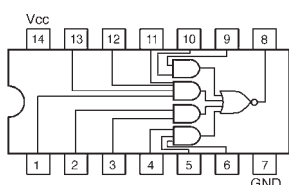
**74 61** triple 3 input expander



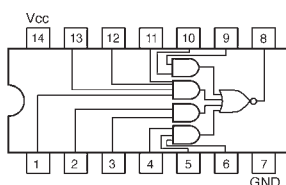
**74 62** 3 2 2 3 input AND OR



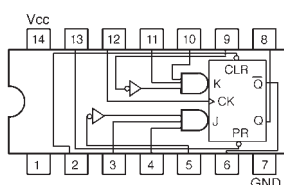
**74 64** 4 2 3 2 input AND OR INV



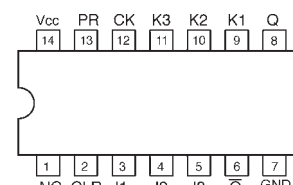
**74 65** 4 2 3 2 input AND OR INV



**74 70** 1 bascule JK à 3 entrées avec R et S



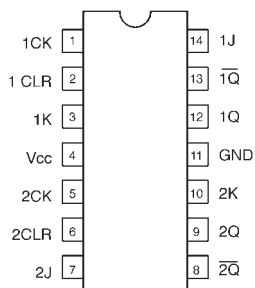
**74 72** 1 bascule JK maître-esclave à 3 entrées avec R et S



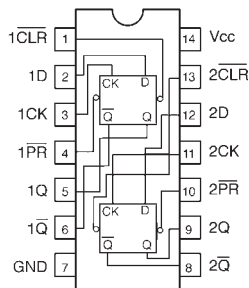
# CIRCUITS INTEGRES



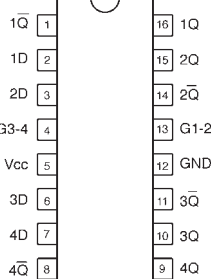
**74 73** 2 bascules JK avec RAZ



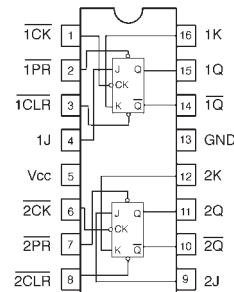
**74 74** 2 bascules D avec R et S



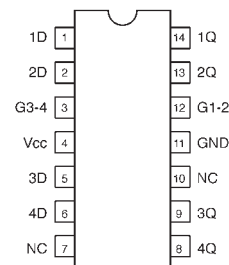
**74 75** 2 doubles bascules à verrouillage



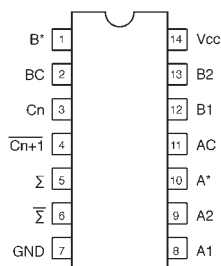
**74 76** 2 bascules JK avec R et S



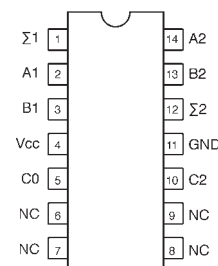
**74 77** verrou 4 bits



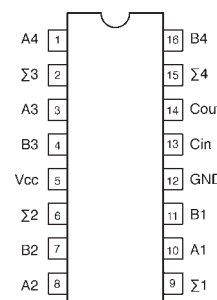
**74 80** additionneur complet 1 bit



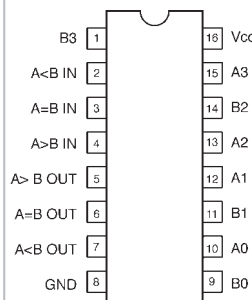
**74 82** additionneur complet 2 bits



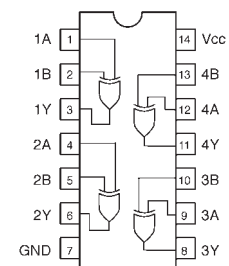
**74 83** additionneur complet 4 bits



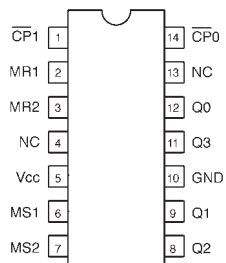
**74 85** comparateur 4 bits



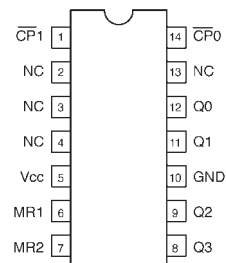
**74 86** 4 portes OU-EXCLUSIF à 2 entrées



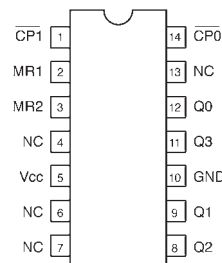
**74 90** compteur décimal



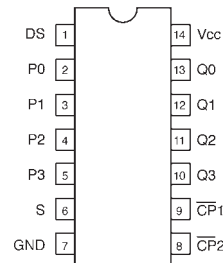
**74 92** compteur hexadécimal



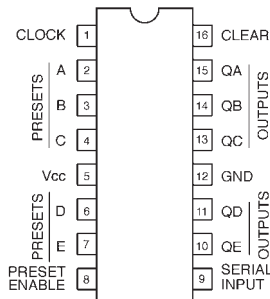
**74 93** compteur binaire asynchrone 4 bits



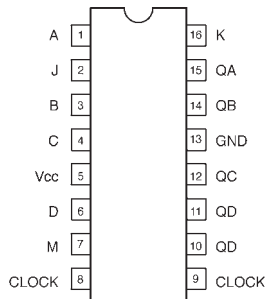
**74 95** registre à décalage 4 bits



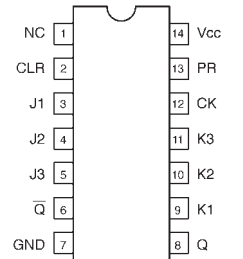
**74 96** registre à décalage 5 bits



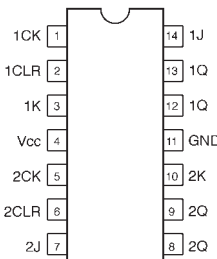
**74 99** 4 bit R shift L shift register



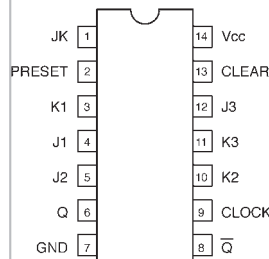
**74 102** 1 bascule JK maître-esclave à 3 entrées avec R et S



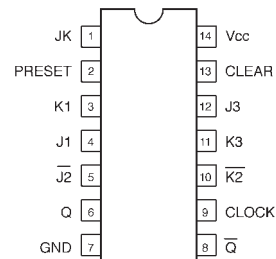
**74 103** JK flip flop



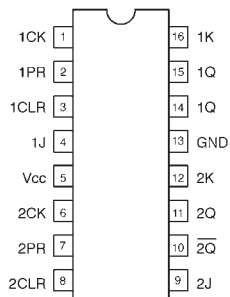
**74 104** 1 bascule JK maître-esclave à 3 entrées avec R et S



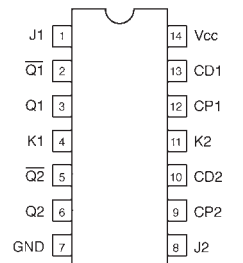
**74 105** 1 bascule JK maître-esclave à 3 entrées avec R et S



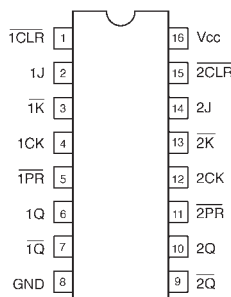
**74 106** dual JK flip flop



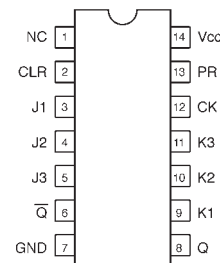
**74.107** 2 bascules JK avec RAZ



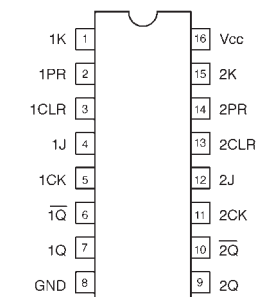
**74 109** 2 bascules JK à déclenchement sur front montant



**74 110** dual JK flip flop with data lockout



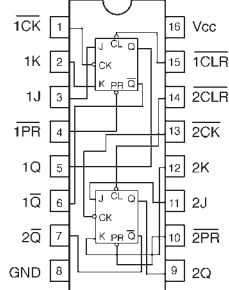
**74 111** 2 bascules JK avec R et S



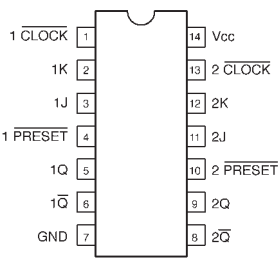


# CIRCUITS INTEGRES

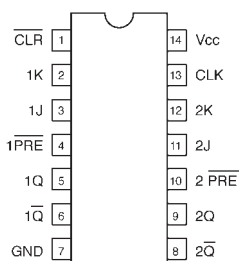
**74 112** 2 bascules JK avec R et S



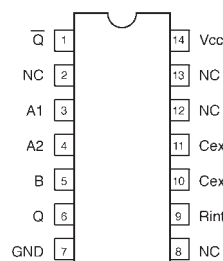
**74 113** 2 bascules JK avec S déclenchement sur front descendant



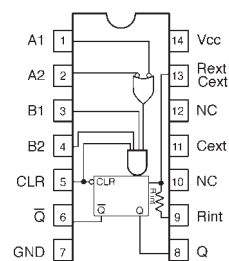
**74 114** dual JK flip flop



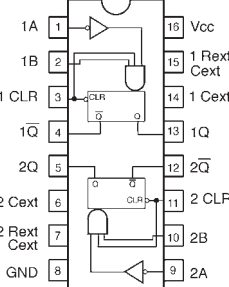
**74 121** monostable multivibrateur avec bascule de schmitt en entrées



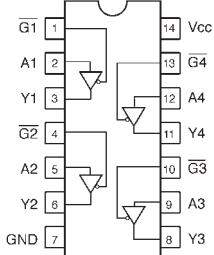
**74 122** monostable redéclenchable avec RAZ



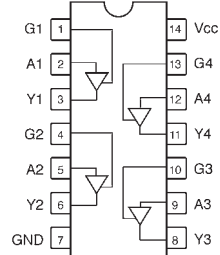
**74 123** 2 multivibrateurs monostables redéclenchables



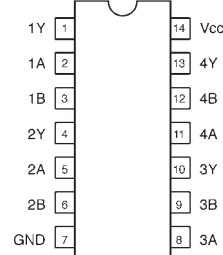
**74 125** 4 amplificateurs 3 états



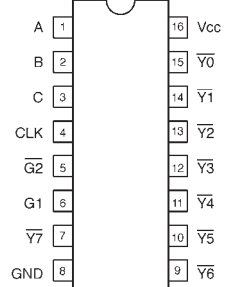
**74 126** 4 amplificateurs 3 états



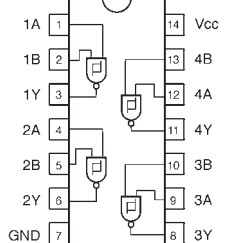
**74 128** 4 portes OU-NON à 2 entrées



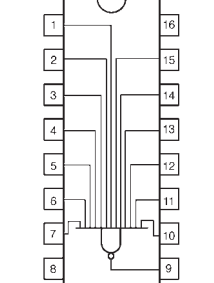
**74 131** 3 line to 8 line decoders/demultiplexers with address registers



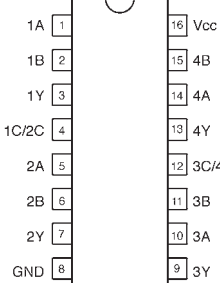
**74 132** 4 portes ET-NON trigger de Schmitt à 2 entrées



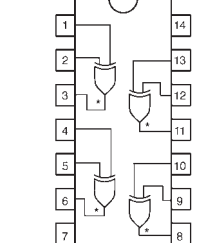
**74 133** 1 porte ET-NON à 13 entrées



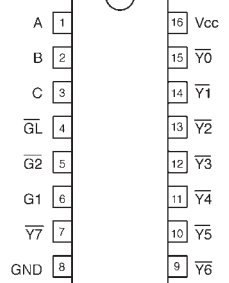
**74 135** quad exclusive OR NOR



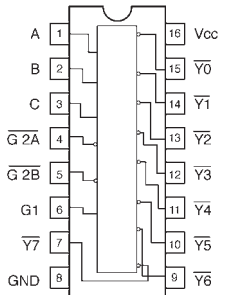
**74 136** 4 portes OU exclusifs à 2 entrées, C.O.



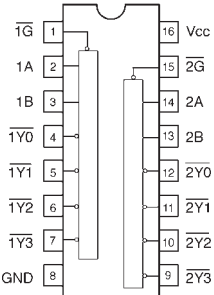
**74 137** 1 décodeur-démultiplexeur 3 vers 8 entrées mémorisées



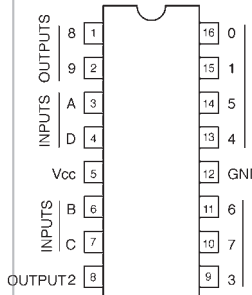
**74 138** 1 décodeur-démultiplexeur 3 vers 8



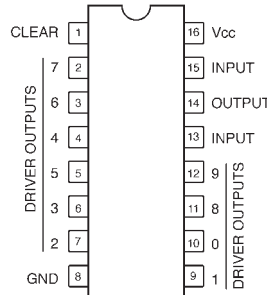
**74 139** 2 décodeurs-démultiplexeurs 2 vers 4



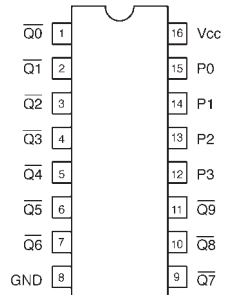
**74 141** décodeur BCD décimal



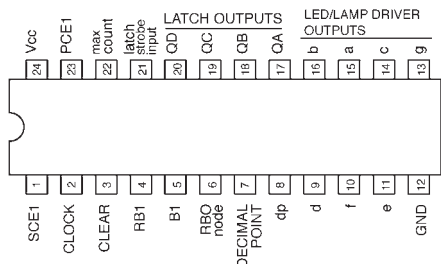
**74 142** BCD counter/latch/decoder/driver



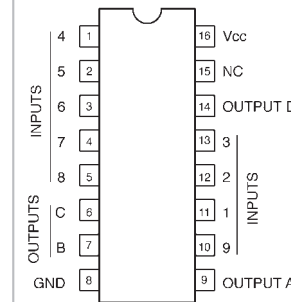
**74 145** 1 décodeur BCD-décimal C.O. (15 V)



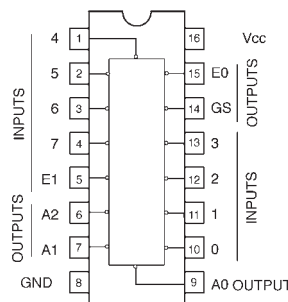
**74 143/74 144** 4 bit counter/latch/7 segment lamp driver



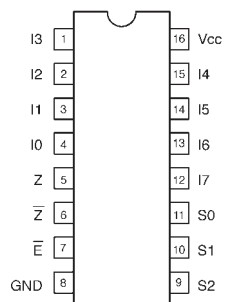
**74 147** 10 to 4 line priority encoder



**74 148** 1 codeur de priorité 8 vers 3



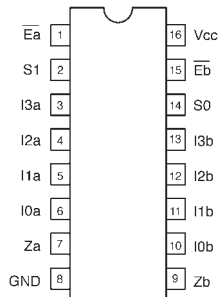
**74 151** 1 multiplexeur 8 vers 1 sorties complémentaires



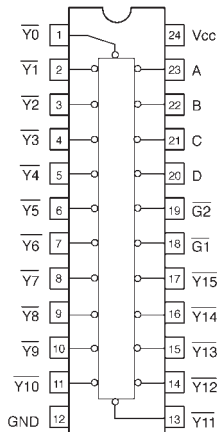
# CIRCUITS INTEGRES



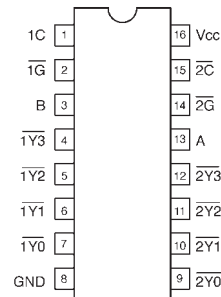
**74 153** Double multiplexeur  
4 vers 1



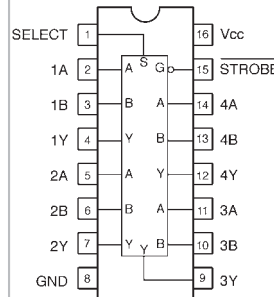
**74 154** décodeur-démultiplexeur  
4 vers 16



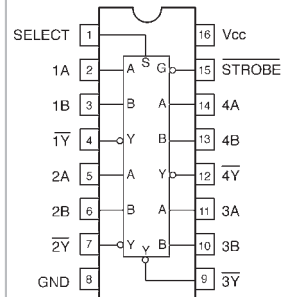
**74 155** double décodeur-démultiplexeur  
2 vers 4



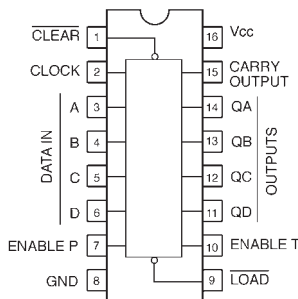
**74 157** quadruple sélecteur-multiplexeur  
2 vers 1



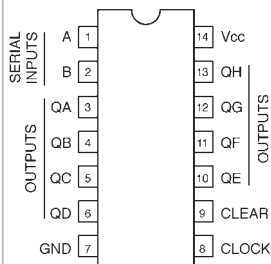
**74 158** quadruple sélecteur-multiplexeur  
2 vers 1



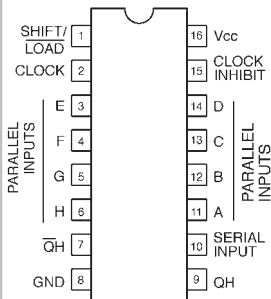
**74 160/161/162/163**  
compteur décimal synchrone



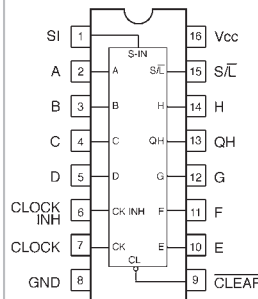
**74 164** registre à décalage 8 bits  
sortie parallèle



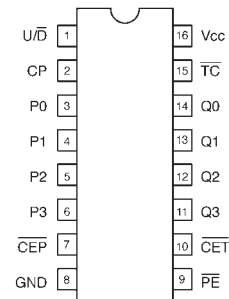
**74 165** registre à décalage 8 bits



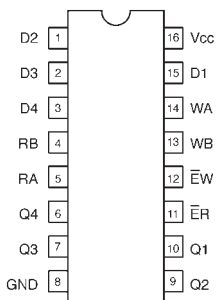
**74 166** registre à décalage 8 bits



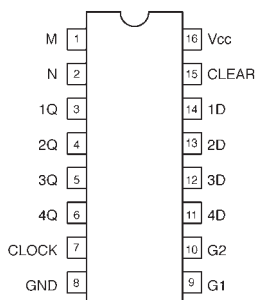
**74 168/74 169**  
compteur - décompteur  
(168 décimal, 169 binaire)



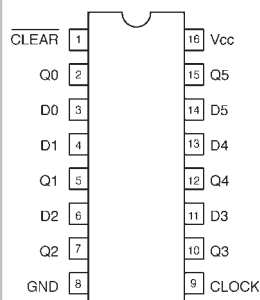
**74 170** registre 4 x 4 bits C.O.



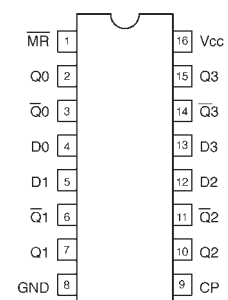
**74 173** registre D 4 bits  
sortie 3 états



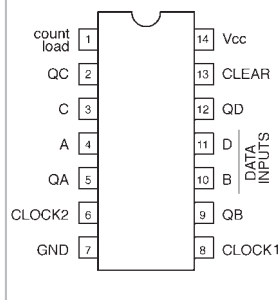
**74 174** sextuple bascule D avec R commune



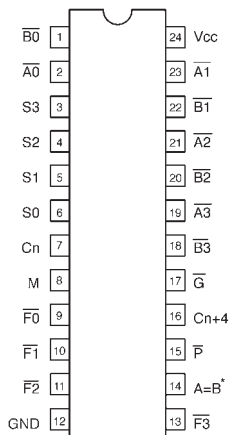
**74 175** quadruple bascule D  
avec R commune



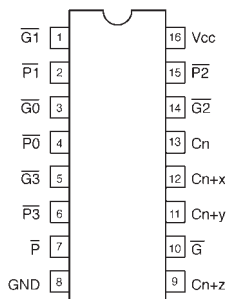
**74 176** compteur décimal  
programmable



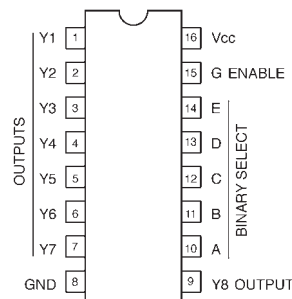
**74 181** ALU 4 bits et générateur  
de fonction



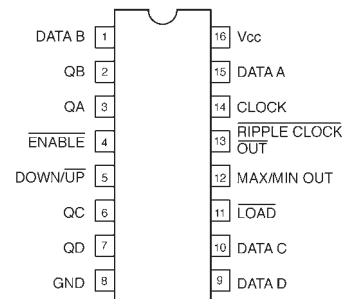
**74 182** générateur de report  
anticipé



**74 184/74 185** BCD binary converter



**74 190/74 191**  
190 : compteur-décompteur BCD synchrone  
191 : compteur-décompteur binaire synchrone



\* open drain output structure

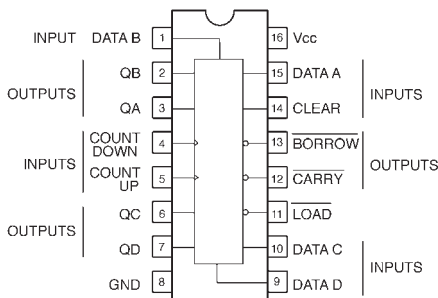




# CIRCUITS INTEGRES

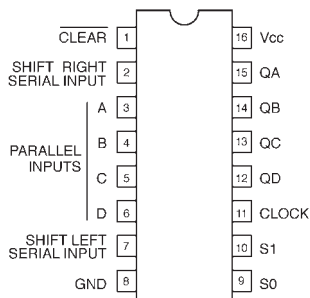
**74 192/74 193**

compteur-décompteur BCD synchrone avec 2 horloges et RAZ



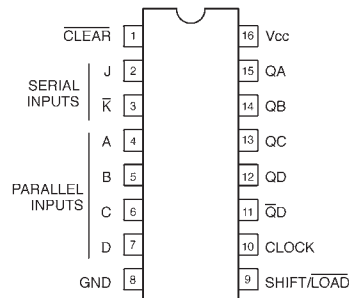
**74 194**

registre à décalage 4 bits bidirectionnel



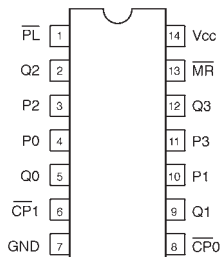
**74 195**

registre à décalage 4 bits

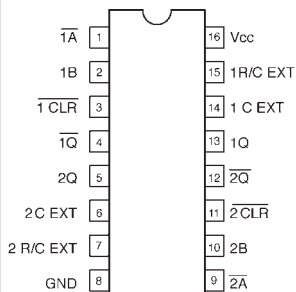


**74 196/74 197**

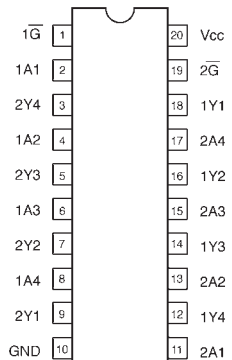
196 : compteur décimal programmable  
197 : compteur binaire 4 bits programmable



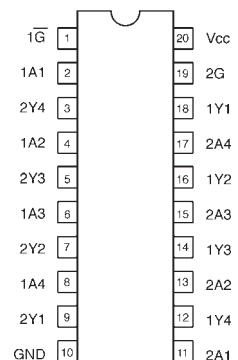
**74 221** 2 monostables avec entrées à bascule de Schmitt et RAZ



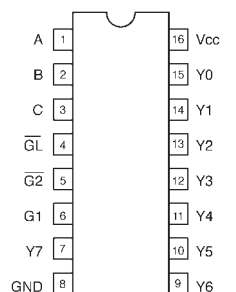
**74 230** octal buffers and line drivers with 3 state outputs



**74 231** octal buffers and line drivers with 3 state outputs

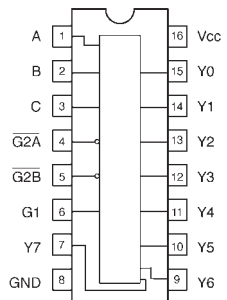


**74 237** décodeur-démultiplexeur 3 vers 8 avec verrou d'adresse

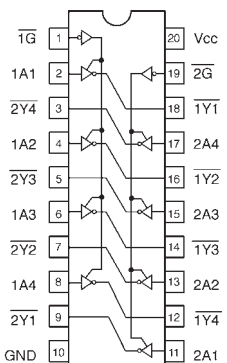


**74 238**

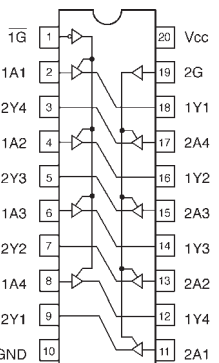
décodeur-démultiplexeur 3 vers 8



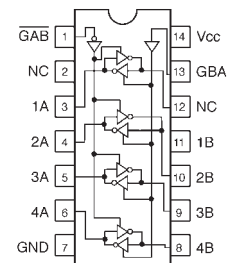
**74 240** 2 quadruples amplificateurs inverseurs de bus, 3 états



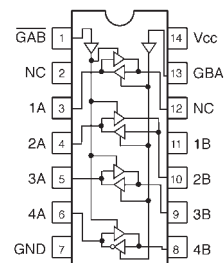
**74 241** 2 quadruples amplificateurs de bus, 3 états



**74 242** quadruple amplificateur-inverseur bidirectionnel, 3 états

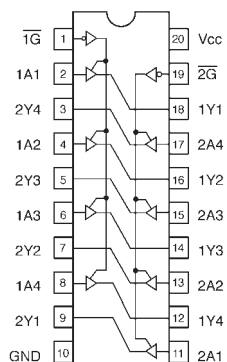


**74 243** quadruple amplificateur bidirectionnel, 3 états

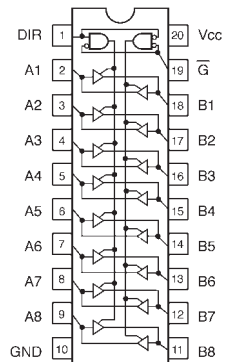


**74 244**

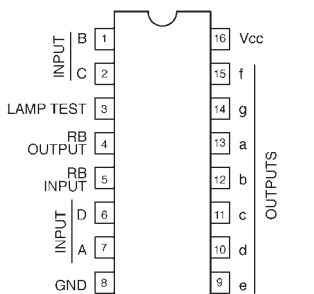
2 quadruples amplificateurs de bus 3 états



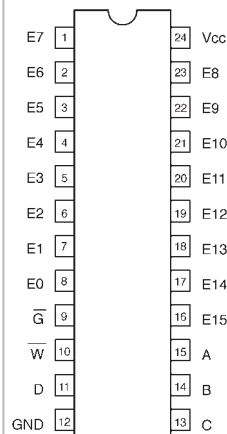
**74 245** octuple amplificateur de bus bidirectionnel, 3 états



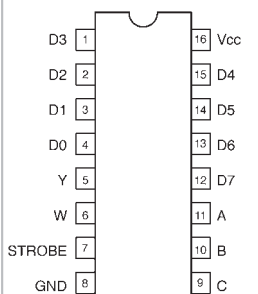
**74 246/74 247** 246 : C.O., 30 V  
**74 248/74 249** 247 : C.O., 15 V  
décodeur BCD-7 segments de commande d'afficheur  
248 : 2 kΩ pull-up de commande d'afficheur  
249 : C.O., 5.5 V



**74 250** 1 of 16 data generators/multiplexers with 3 state outputs

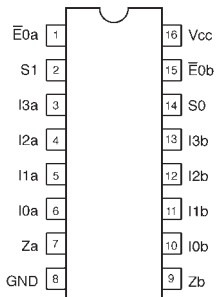


**74 251** sélecteur-multiplexeur 8 vers 1 avec sorties 3 états

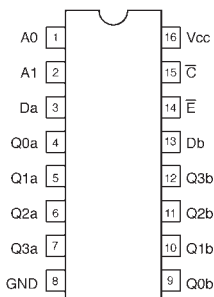




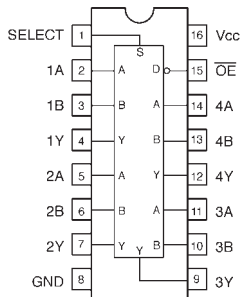
double sélecteur-multiplexeur  
**74 253** 4 vers 1 avec sorties 3 états



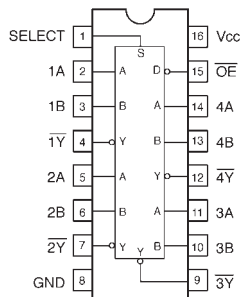
**74 256**  
dual 4 bit addressable latch



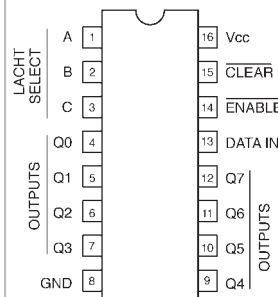
**74 257**  
quadruple sélecteur-multiplexeur  
2 vers 1 avec sorties 3 états



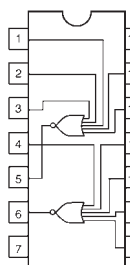
**74 258**  
quadruple sélecteur-multiplexeur  
2 vers 1 avec sorties 3 états



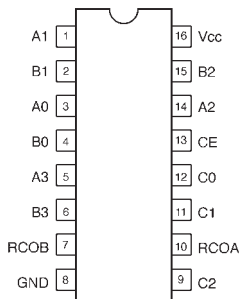
**74 259** octuple verrou adressable  
avec validation et RAZ



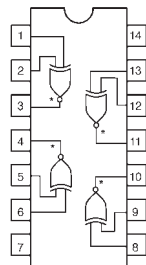
**74 260**  
dual 5 input nor gate



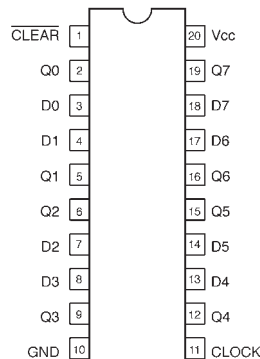
look-ahead carry generators  
for counters  
**74 264**



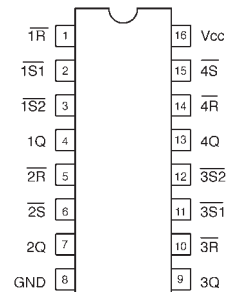
**74 266** 4 portes  
OU-NON EXCLUSIF  
à 2 entrées C.O.



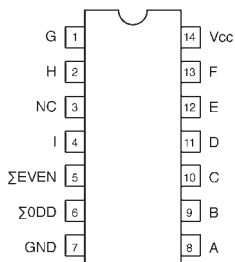
**74 273** octal D type flip-flops  
with clear



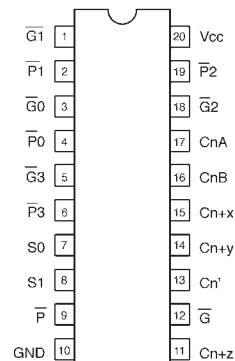
**74 279** quad set-reset latch



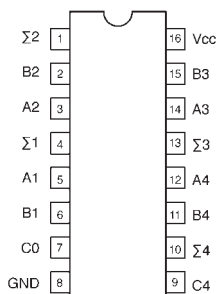
générateur-contrôleur  
de parité 9 bits  
**74 280**



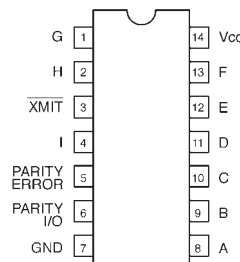
look-ahead carry generator with  
selectable carry inputs  
**74 282**



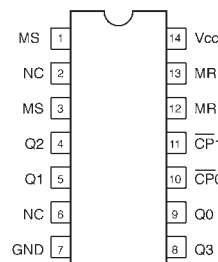
**74 283**  
additionneur complet 4 bits



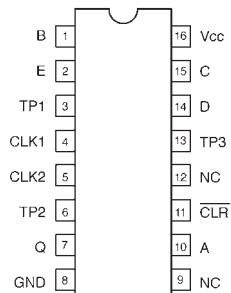
**74 286**  
9 bit parity generators/checker  
with bus driver parity I/O port



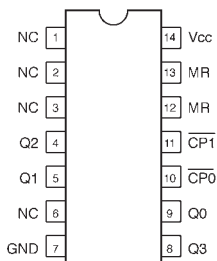
**74 290** compteur décimal



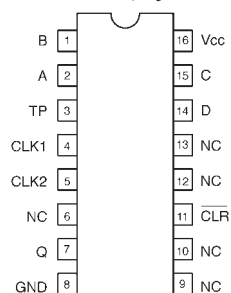
diviseur de  
fréquence-temporisateur  
programmable  
**74 292**



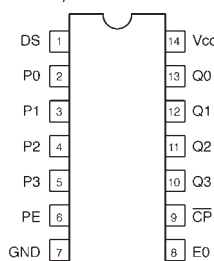
compteur binaire  
asynchrone 4 bits  
**74 293**



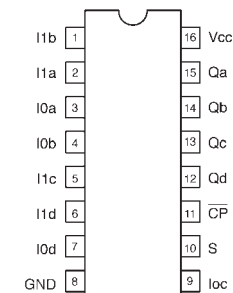
diviseur de  
fréquence-temporisateur  
programmable  
**74 294**



**74 295** registre à décalage  
4 bits avec entrées et sorties  
en parallèle sortie 3 états



quadruple sélecteur-multiplexeur  
**74 298** 2 vers 1 avec mémoire

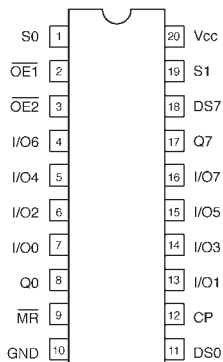




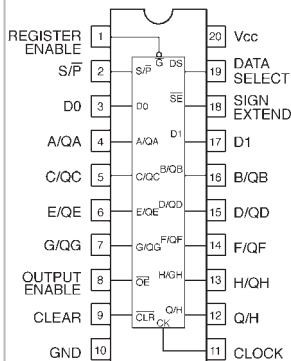


# CIRCUITS INTEGRES

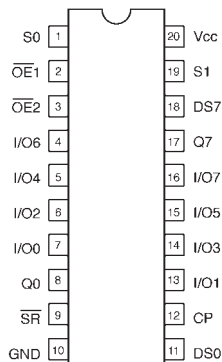
**74 299** registre à décalage universel 8 bits sortie 3 états



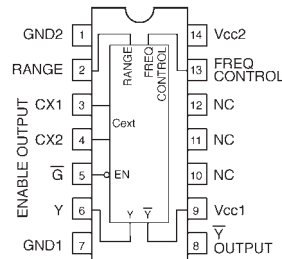
**74 322** 8 bit shift registers with sign extend



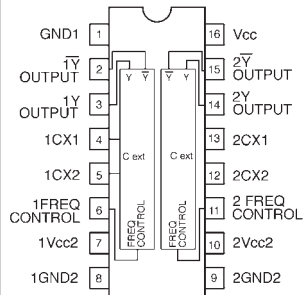
**74 323** registre à décalage universel 8 bits, sortie 3 états



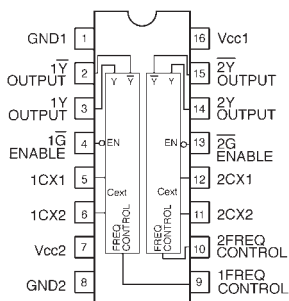
**74 324** voltage-controlled oscillators



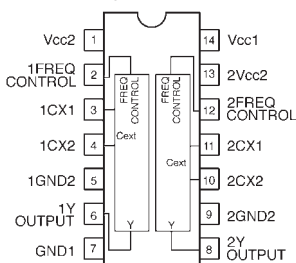
**74 325** voltage-controlled oscillators



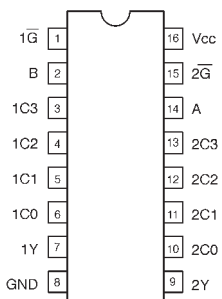
**74 326** voltage-controlled oscillators



**74 327** voltage-controlled oscillators

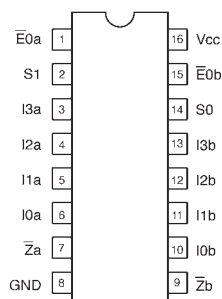


double sélecteur-multiplexeur **74 352** 4 vers 1

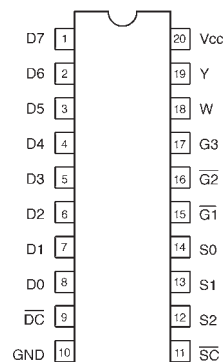


**74 353**

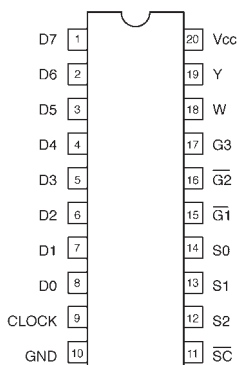
double sélecteur-multiplexeur 4 vers 1 avec sorties 3 états



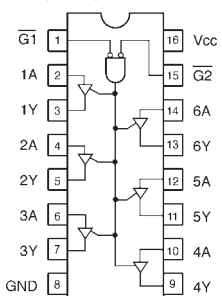
sélecteur-multiplexeur 8 vers 1 **74 354** avec registre d'entrée



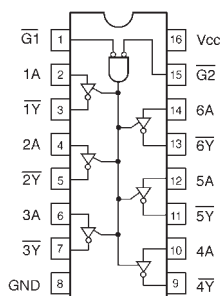
sélecteur-multiplexeur 8 vers 1 **74 356** avec registre d'entrée



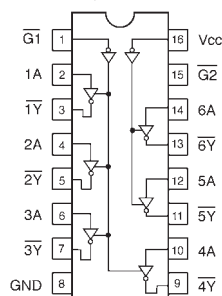
**74 365** sextuple amplificateur, 3 états



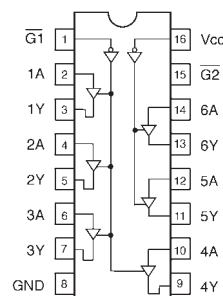
sextuple amplificateur inverseur **74 366** 3 états



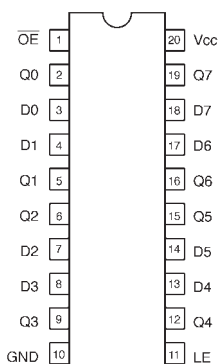
**74 367** double et quadruple amplificateurs, 3 états



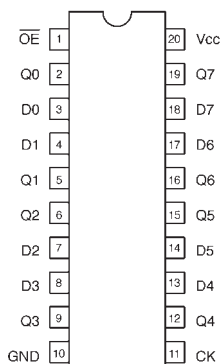
**74 368** double et quadruple amplificateurs inverseurs, 3 états



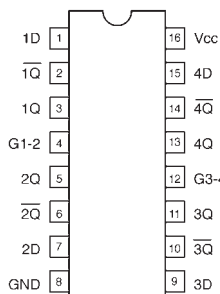
**74 373** octuple verrou, 3 états



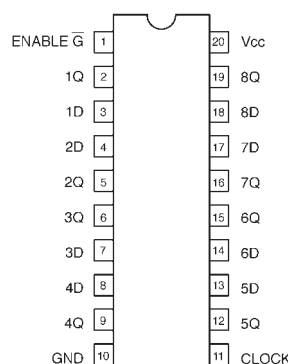
**74 374** octuple bascule D sortie 3 états



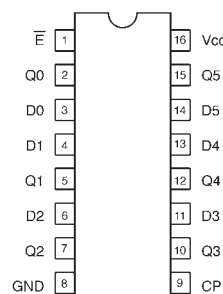
**74 375** 2 doubles bascules à verrouillage



**74 377** octuple bascule D avec entrée de validation

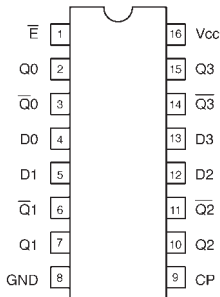


**74 378** sextuple bascule D avec entrée validation

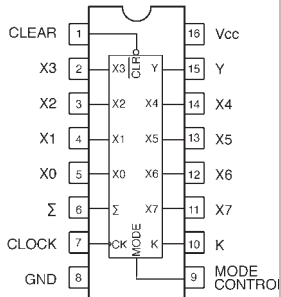




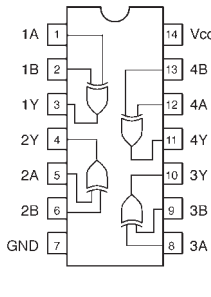
**74 379** quadruple bascule D avec entrée de validation



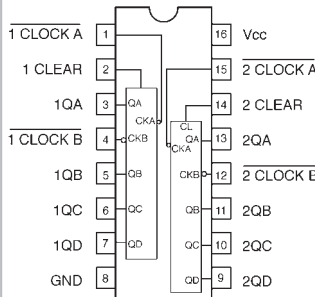
**74 384** 8 bit by 1 bit two's-complement multiplieur



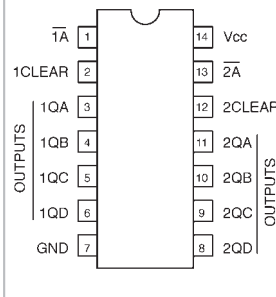
**74 386** 4 portes OU-EXCLUSIF à 2 entrées



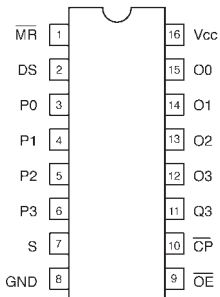
**74 390** 2 compteurs décimaux



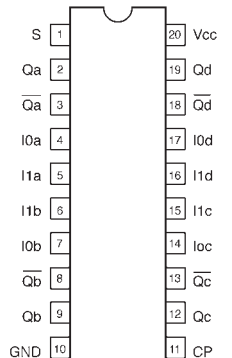
**74 393** 2 compteurs binaires 4 bits



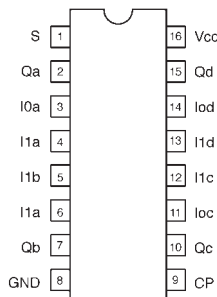
**74 395** registre à décalage 4 bits avec entrées et sorties en parallèle, sortie 3 états



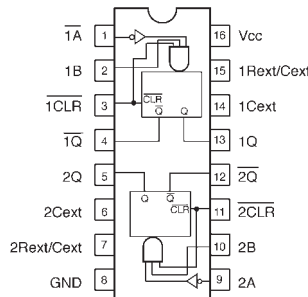
**74 398** quadruple sélecteur-multiplexeur 2 vers 1 avec mémoire



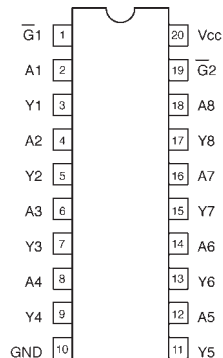
**74 399** quadruple sélecteur-multiplexeur 2 vers 1 avec mémoire



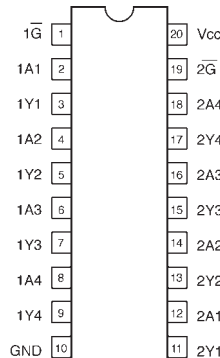
**74 423** 2 monostables redéclençables avec RAZ



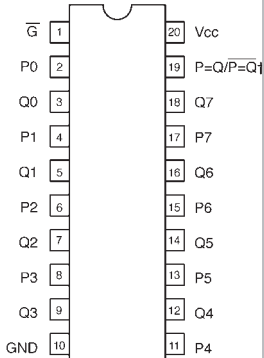
**74 465/74 466** octuple amplificateur 3 états



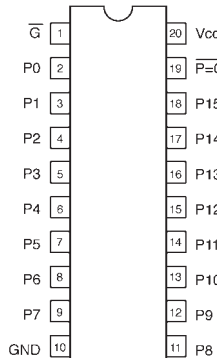
**74 467/74 468** 2 quadruples amplificateurs de bus 3 états



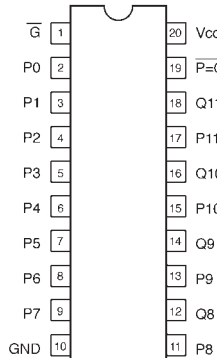
**74 518/74 522** 8 bit identity comparators



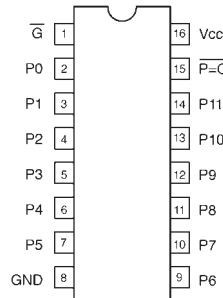
**74 526** fuse programmable identity comparators



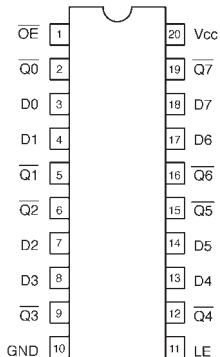
**74 527** fuse programmable identity comparators



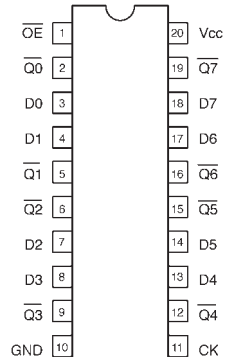
**74 528** fuse programmable identity comparators



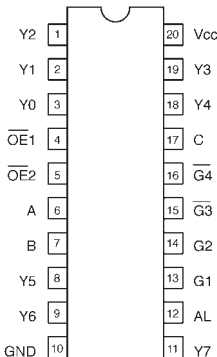
**74 533** octuple verrou inverseur 3 états



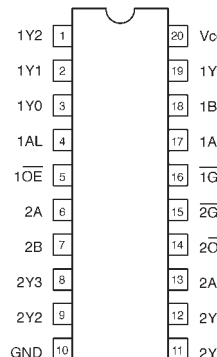
**74 534** octuple bascule D sortie inversée 3 états



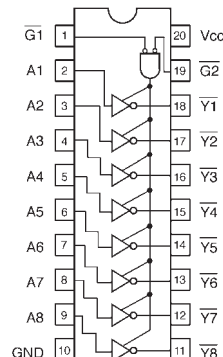
**74 538** 3 line to 8 line decoders/demultiplexers with 3 state outputs



**74 539** dual 2 line to 4 line decoders/demultiplexers with 3 state outputs



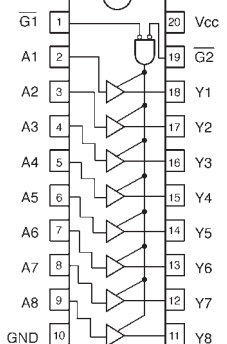
**74 540** octuples amplificateurs inverseurs de bus 3 états



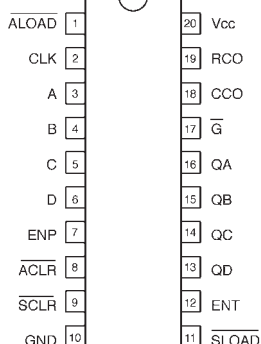


# CIRCUITS INTEGRES

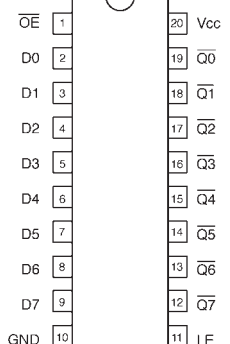
**74 541** octuple amplificateur 3 états



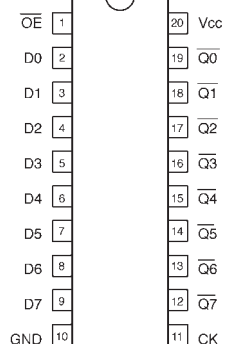
**74 560/74 561** synchronous 4 bit counters with 3 state outputs



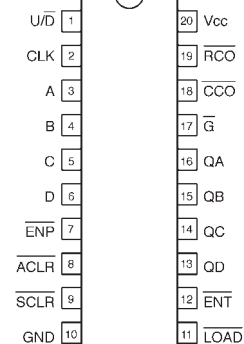
**74 563** octuple verrou inverseur 3 états



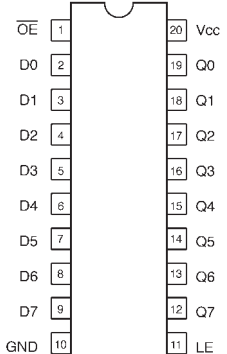
**74 564** octuple bascule D sortie inversée 3 états



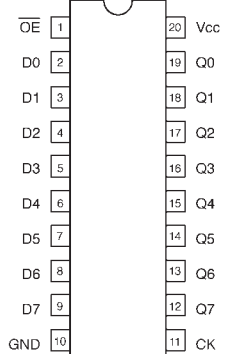
**74 568/74 569** synchronous 4 bit up/down decade and binary counters with 3 state outputs



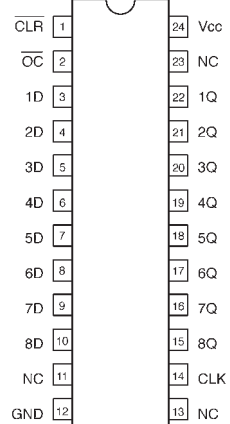
**74 573** octuple verrou 3 états



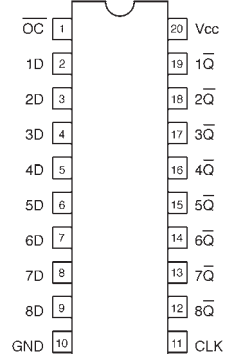
**74 574** octuple bascule D sortie 3 états



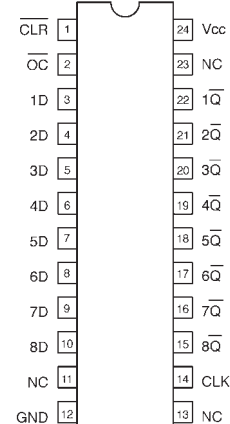
**74 575** octuple bascule D sortie 3 états



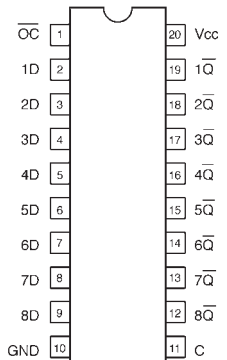
**74 576** octuple bascule D sortie 3 états



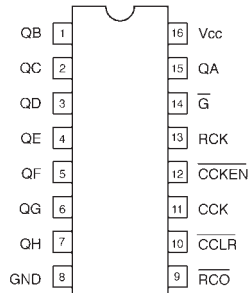
**74 577** octuple bascule D sortie 3 états



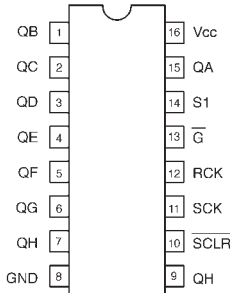
**74 580** octal D type transparent latches



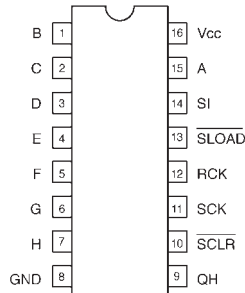
**74 590** compteur binaire 8 bits avec registre



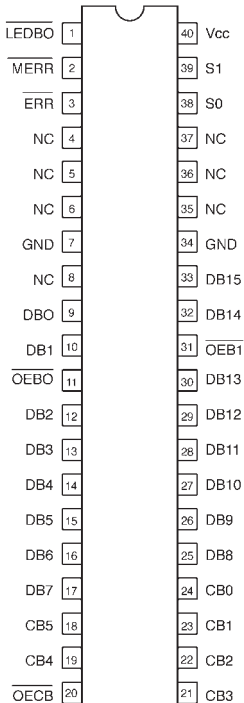
**74 595** registre à décalage 8 bits avec registre de sortie



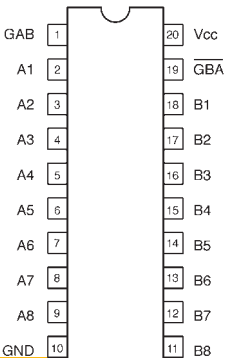
**74 597** registre à décalage 8 bits avec registre d'entrée



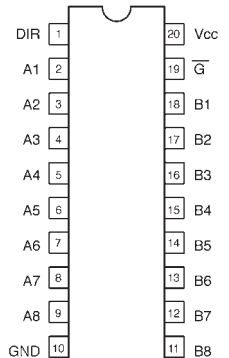
**74 616/74 617** 16 bit parallel error detection and correction circuits



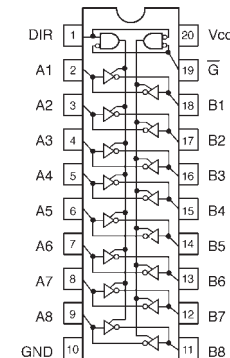
**74 620/74 623** octuple amplificateur de bus bidirectionnel, 3 états



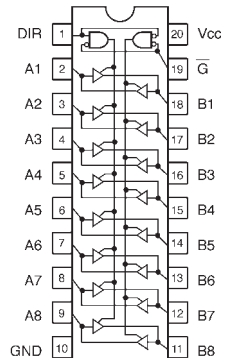
**74 638/74 639** octuple amplificateur-inverseur bidirectionnel, 3 états C.O.



**74 640** octuple amplificateur-inverseur de bus bidirectionnel, 3 états



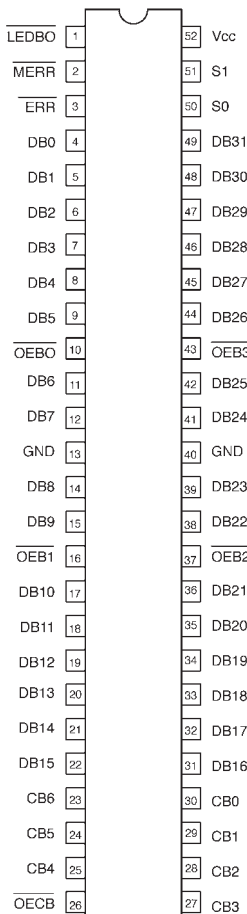
**74 641** octuple amplificateur de bus bidirectionnel C.O.





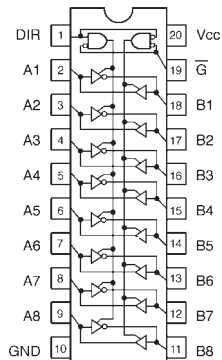
### 74 632/74 633

32 bit parallel error detection and correction circuits



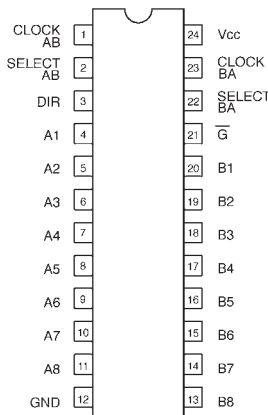
### 74 643

octuple amplificateur inverseur non inverseur, bidirectionnel



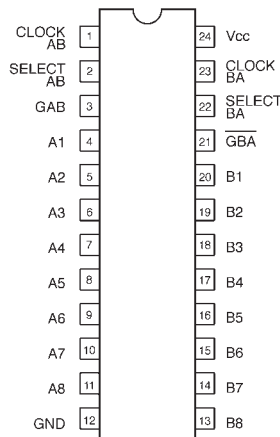
### 74 646...74 649

octuple amplificateur de bus bidirectionnel avec registre



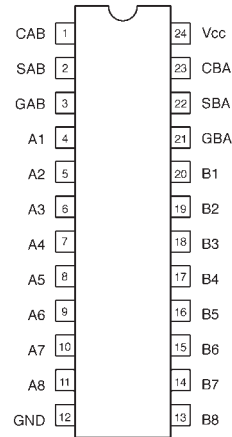
### 74 651/74 652

octuple amplificateur de bus bidirectionnel avec registre

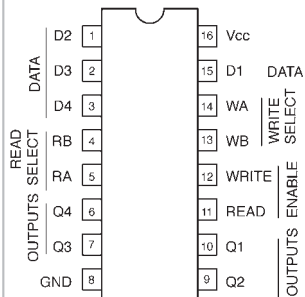


### 74 654

octuple amplificateur de bus bidirectionnel avec registre

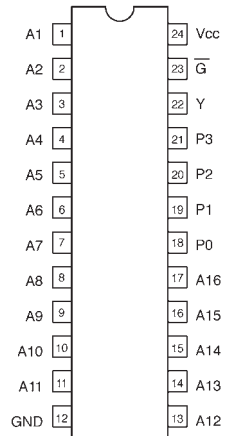


### 74 670 registre 4 x 4 bits, sorties 3 états



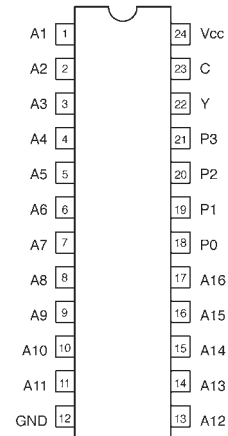
### 74 677

comparateur d'adresses 16 bits



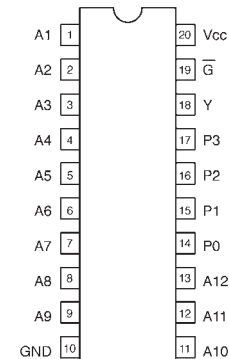
### 74 678

comparateur d'adresses 16 bits



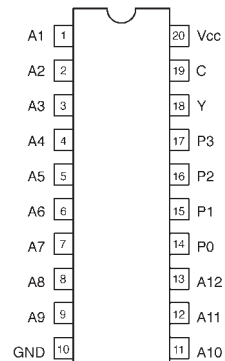
### 74 679

comparateur d'adresses 12 bits



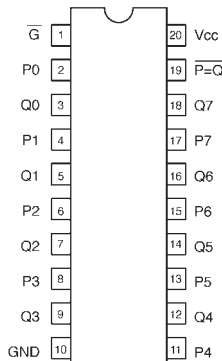
### 74 680

comparateur d'adresses 12 bits



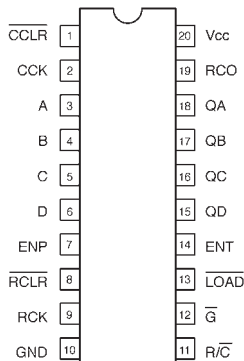
### 74 688/74 689

comparateur 8 bits



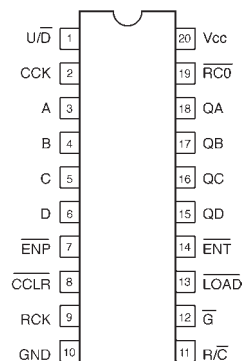
### 74 690...74 693

compteur synchrone 4 bits avec registre et multiplexeur



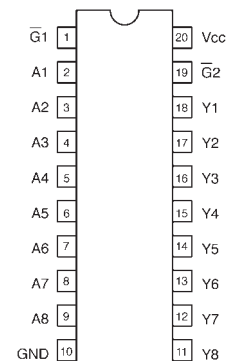
### 74 696/74 697

compteur-décompteur synchrone 4 bits avec registre et multiplexeur



### 74 746/74 747

octal buffers and line drivers with input pull-up resistors





# CIRCUITS INTEGRES

## CIRCUIT INTEGRE TTL

série 74 HC

CODE	DÉSIGNATION		1	10	25
74 HC 00	DIP 14	Quad 2-input NAND gate	0.34	0.26	0.22
74 HC 02	DIP 14	Quad 2-input NOR gate	0.34	0.26	0.22
74 HC 03	DIP 14	Quad 2-input NAND gate	0.46	0.35	0.30
74 HC 04	DIP 14	Hex inverter	0.34	0.26	0.22
74 HCU 04	DIP 14	Hex inverter	0.73	0.55	0.47
74 HC 05	DIP 14	Hex Inverter w-O/C Output	0.37	0.28	0.24
74 HC 08	DIP 14	Quad 2-input AND gate	0.34	0.26	0.22
74 HC 10	DIP 14	Triple 3-input NAND gate	0.34	0.26	0.22
74 HC 11	DIP 14	Triple 3-input AND gate	0.76	0.57	0.49
74 HC 14	DIP 14	Hex inverting Schmitt trigger	0.43	0.32	0.28
74 HC 20	DIP 14	Dual 4-input NAND gate	0.37	0.28	0.24
74 HC 21	DIP 14	Dual 4-input AND gate	0.55	0.41	0.36
74 HC 27	DIP 14	Triple 3-input NOR gate	0.40	0.30	0.26
74 HC 30	DIP 14	8-input NAND gate	0.61	0.46	0.40
74 HC 32	DIP 14	Quad 2-input NAND Schmitt trigger	0.31	0.23	0.20
74 HC 42	DIP 16	BCD to decimal decoder (1-of-10)	0.67	0.50	0.44
74 HC 51	DIP 14	Dual 2-Input AND-OR Inverter Gates	0.56	0.42	0.36
74 HC 58	DIP 14	Dual AND-OR gate	0.67	0.50	0.44
74 HC 73	DIP 14	Dual JK flip-flop with reset; negative-edge trigger	0.61	0.46	0.40
74 HC 74	DIP 14	Dual D-type flip-flop with set and reset; positive-edge trigger	0.34	0.26	0.22
74 HC 75	DIP 16	Quad bistable transparent latch	0.82	0.61	0.53
74 HC 76	DIP 16	Dual J-K flip flop + pset/clear	0.85	0.64	0.55
74 HC 85	DIP 16	4-bit magnitude comparator	1.07	0.80	0.70
74 HC 86	DIP 14	Quad 2-input EXCLUSIVE-OR gate	0.46	0.35	0.30
74 HC 107	DIP 14	Dual JK flip-flop with reset; negative-edge trigger	0.85	0.64	0.55
74 HC 109	DIP 16	Description : Dual JK flip-flop with set and reset; positive-edge trigger	0.61	0.46	0.40
74 HC 112	DIP 16	Dual JK flip-flop with set and reset; negative-edge trigger	0.64	0.48	0.42
74 HC 123	DIP 16	Dual retriggerable monostable multivibrator with reset	0.92	0.69	0.60
74 HC 125	DIP 14	Quad buffer/line driver; 3-state	0.61	0.46	0.40
74 HC 126	DIP 14	Quad buffer/line driver; 3-state	0.92	0.69	0.60
74 HC 132	DIP 14	Quad 2-input NAND Schmitt trigger	0.40	0.30	0.26
74 HC 137	DIP 16	3-to-8 line decoder/demultiplexer with address latches; inverting	1.07	0.80	0.70
74 HC 138	DIP 16	3-to-8 line decoder/demultiplexer; inverting	0.61	0.46	0.40
74 HC 139	DIP 16	Dual 2-to-4 line decoder/demultiplexer	0.61	0.46	0.40
74 HC 147	DIP 16	10-to-4 line priority encoder	1.07	0.80	0.70
74 HC 148	DIP 16	8-input priority encoder	1.07	0.80	0.70
74 HC 151	DIP 16	8-input multiplexer	0.76	0.57	0.49
74 HC 153	DIP 16	Dual 4-input multiplexer	0.61	0.46	0.40
74 HC 154	DIP 24	4-to-16 line decoder/demultiplexer (entraxe 7.62)	1.07	0.80	0.70
74 HC 154 P15	DIP 24	4-to-16 line decoder/demultiplexer (entraxe 15.24)	1.68	1.26	1.09
74 HC 157	DIP 16	Quad 2-input multiplexer	0.95	0.71	0.62
74 HC 158	DIP 16	Quad 2-input multiplexer; inverting	0.70	0.52	0.45
74 HC 160	DIP 16	Presetable synchronous BCD decade counter; asynchronous reset	0.92	0.69	0.60
74 HC 161	DIP 16	Presetable synchronous 4-bit binary counter; asynchronous reset	0.76	0.57	0.49
74 HC 162	DIP 16	Presetable synchronous BCD decade counter; synchronous reset	1.22	0.92	0.79
74 HC 163	DIP 16	Presetable synchronous 4-bit binary counter; synchronous reset	0.92	0.69	0.60
74 HC 164	DIP 14	8-bit serial-in/parallel-out shift register	0.70	0.52	0.45
74 HC 165	DIP 16	8-bit parallel-in/serial-out shift register	0.92	0.69	0.60
74 HC 166	DIP 16	8-bit parallel-in/serial-out shift register	0.76	0.57	0.49
74 HC 173	DIP 16	Quad D-type flip-flop; positive-edge trigger; 3-state	1.53	1.15	0.99
74 HC 174	DIP 16	Hex D-type flip-flop with reset; positive-edge trigger	0.76	0.57	0.49
74 HC 175	DIP 16	Quad D-type flip-flop with reset; positive-edge trigger	0.61	0.46	0.40
74 HC 190	DIP 16	Presetable Synchronous BCD Decade Up/Down Counter	0.85	0.64	0.55
74 HC 191	DIP 16	Presetable synchronous 4-bit binary up/down counter	0.85	0.64	0.55
74 HC 192	DIP 16	Decade Up/Down Counter with Clear	1.22	0.92	0.79
74 HC 193	DIP 16	Presetable synchronous 4-bit binary up/down counter	0.92	0.69	0.60
74 HC 194	DIP 16	4-bit bidirectional universal shift register	1.53	1.15	0.99
74 HC 195	DIP 16	4 bit parallel-access shift register	0.85	0.64	0.55

série 74



# CIRCUITS INTEGRES



## CIRCUIT INTEGRE TTL

série 74 HC

CODE	DÉSIGNATION	1	10	25
74 HC 221	DIP 16 Dual non-retriggerable monostable multivibrator with reset	0.85	0.64	0.55
74 HC 237	DIP 16 3-to-8 line decoder/demultiplexer with address latches	0.85	0.64	0.55
74 HC 238	DIP 16 3-to-8 line decoder/demultiplexer	0.67	0.50	0.44
74 HC 240	DIP 20 Octal buffer/line driver; 3-state; inverting	0.61	0.46	0.40
74 HC 241	DIP 20 Octal buffer/line driver; 3-state	1.83	1.37	1.19
74 HC 242	DIP 14 Inverting Quad Tri-State Transceiver	0.67	0.50	0.44
74 HC 243	DIP 14 Quad bus transceiver; 3-state	2.09	1.57	1.36
74 HC 244	DIP 20 Octal buffer/line driver; 3-state	0.70	0.52	0.45
74 HC 245	DIP 20 Octal bus transceiver; 3-state	0.70	0.52	0.45
74 HC 251	DIP 16 8-input multiplexer; 3-state	1.22	0.92	0.79
74 HC 253	DIP 16 Dual 4-input multiplexer; 3-state	0.79	0.59	0.51
74 HC 257	DIP 16 Quad 2-input multiplexer; 3-state	0.70	0.52	0.45
74 HC 259	DIP 16 8-bit addressable latch	1.22	0.92	0.79
74 HC 273	DIP 20 Octal D-type flip-flop with reset; positive-edge trigger	0.85	0.64	0.55
74 HC 280	DIP 14 9-bit odd/even parity generator/checker	1.22	0.92	0.79
74 HC 283	DIP 16 4-bit binary full adder with fast carry	1.02	0.76	0.66
74 HC 297	DIP 16 High Speed CMOS Logic Digital Phase-Locked-Loop	2.48	1.86	1.61
74 HC 299	DIP 20 8-bit universal shift register; 3-state	1.37	1.03	0.89
74 HC 365	DIP 16 Hex buffer/line driver; 3-state	0.76	0.57	0.49
74 HC 366	DIP 16 Hex buffer/line driver; 3-state; inverting	1.06	0.79	0.69
74 HC 367	DIP 16 Hex buffer/line driver; 3-state	0.76	0.57	0.49
74 HC 373	DIP 20 Octal D-type transparent latch; 3-state	0.70	0.52	0.45
74 HC 374	DIP 20 Octal D-type flip-flop; positive edge-trigger; 3-state	0.76	0.57	0.49
74 HC 377	DIP 20 Octal D-type flip-flop with data enable; positive-edge trigger	0.92	0.69	0.60
74 HC 390	DIP 16 Dual decade ripple counter	1.04	0.78	0.68
74 HC 393	DIP 14 Dual 4-bit binary ripple counter	0.92	0.69	0.60
74 HC 540	DIP 20 Octal buffer/line driver; 3-state; inverting	0.61	0.46	0.40
74 HC 541	DIP 20 Octal buffer/line driver; 3-state	0.70	0.52	0.45
74 HC 563	DIP 20 Octal D-type transparent latch; 3-state; inverting	1.28	0.96	0.83
74 HC 573	DIP 20 Octal D-type transparent latch; 3-state	0.67	0.50	0.44
74 HC 574	DIP 20 Octal D-type flip-flop; positive edge-trigger; 3-state	0.67	0.50	0.44
74 HC 590	DIP 16 8-bit binary counter w/ output register tri-state	1.07	0.80	0.70
74 HC 595	DIP 16 8-bit serial-in/serial or parallel-out shift register with output latches; 3-state	1.07	0.80	0.70
74 HC 640	DIP 20 Octal bus transceiver; 3-state; inverting	1.53	1.15	0.99
74 HC 643	DIP 20 Octal bus transceiver	1.53	1.15	0.99
74 HC 688	DIP 20 8-bit magnitude comparator	0.85	0.64	0.55
74 HC 4017	DIP 16 Johnson decade counter with 10 decoded outputs	0.92	0.69	0.64
74 HC 4020	DIP 16 14-stage binary ripple counter	1.34	1.01	0.94
74 HC 4024	DIP 14 7-stage binary ripple counter	0.92	0.69	0.64
74 HC 4040	DIP 16 12-stage binary ripple counter	0.76	0.57	0.53
74 HC 4046	DIP 16 Phase Lock Loop	1.68	1.26	1.09
74 HC 4049	DIP 16 Hex inverting high-to-low level shifter	0.67	0.50	0.47
74 HC 4050	DIP 16 Hex high-to-low level shifter	1.25	0.94	0.88
74 HC 4051	DIP 16 8-channel analog multiplexer/demultiplexer	1.53	1.15	1.07
74 HC 4052	DIP 16 Dual 4-channel analog multiplexer/demultiplexer	0.85	0.64	0.60
74 HC 4053	DIP 16 Triple 2-channel analog multiplexer/demultiplexer	1.22	0.92	0.85
74 HC 4060	DIP 16 14-stage binary ripple counter with oscillator	0.67	0.50	0.47
74 HC 4066	DIP 14 Quad bilateral switches	0.79	0.59	0.55
74 HC 4067	DIP 24 16-channel analog multiplexer/demultiplexer	1.66	1.24	1.16
74 HC 4075	DIP 14 Triple 3-input OR gate	0.46	0.35	0.32
74 HC 4078	DIP 14 8-In NOR Gate	0.46	0.35	0.32
74 HC 4094	DIP 16 8-stage shift-and-store bus register	1.53	1.15	1.07
74 HC 4316	DIP 16 Quad bilateral switches	1.04	0.78	0.73

série 74





# CIRCUITS INTEGRES

## CIRCUIT INTEGRE TTL

série 74 HC

CODE	DÉSIGNATION		1	10	25
74 HC 4510	DIP 16	BCD up/down counter	1.13	0.85	0.79
74 HC 4511	DIP 16	BCD to 7-segment latch/decoder/driver	3.66	2.75	2.56
74 HC 4516	DIP 16	Binary up/down counter	2.14	1.61	1.50
74 HC 4520	DIP 16	Dual 4-bit synchronous binary counter	0.92	0.69	0.64
74 HC 4538	DIP 16	Dual retriggerable precision monostable multivibrator	1.22	0.92	0.85
74 HC 4543	DIP 16	BCD to 7-Seg LCD Latch Decoder Driver	1.40	1.05	0.98

## CIRCUIT INTEGRE TTL

série 74 HCT

CODE	DÉSIGNATION		1	10	25
74 HCT 00	DIP 14	Quad 2-input NAND gate	0.31	0.23	0.20
74 HCT 02	DIP 14	Quad 2-input NOR gate	0.34	0.26	0.22
74 HCT 03	DIP 14	Quad 2-input NAND gate	0.34	0.26	0.22
74 HCT 04	DIP 14	Hex inverter	0.31	0.23	0.20
74 HCT 05	DIP 14	Hex Inverter (Open Drain)			
74 HCT 08	DIP 14	Quad 2-input AND gate	0.31	0.23	0.20
74 HCT 10	DIP 14	Triple 3-input NAND gate	0.38	0.28	0.25
74 HCT 11	DIP 14	Triple 3-input AND gate	0.38	0.28	0.25
74 HCT 14	DIP 14	Hex inverting Schmitt trigger	0.38	0.28	0.25
74 HCT 20	DIP 14	Dual 4-input NAND gate	0.43	0.32	0.28
74 HCT 21	DIP 14	Dual 4-input AND gate	0.40	0.30	0.26
74 HCT 27	DIP 14	Triple 3-input NOR gate	0.46	0.35	0.30
74 HCT 30	DIP 14	8-input NAND gate	0.61	0.46	0.40
74 HCT 32	DIP 14	Quad 2-input OR gate	0.46	0.35	0.30
74 HCT 42	DIP 16	BCD to decimal decoder (1-of-10)	0.92	0.69	0.60
74 HCT 73	DIP 14	Dual JK flip-flop with reset; negative-edge trigger	0.76	0.57	0.49
74 HCT 74	DIP 14	Dual D-type flip-flop with set and reset; positive-edge trigger	0.55	0.41	0.36
74 HCT 85	DIP 16	4-bit magnitude comparator	0.79	0.59	0.51
74 HCT 86	DIP 14	Quad 2-input EXCLUSIVE-OR gate	0.76	0.57	0.49
74 HCT 93	DIP 14	4-bit binary ripple counter	1.22	0.92	0.79
74 HCT 107	DIP 14	Dual JK flip-flop with reset; negative-edge trigger	0.46	0.35	0.30
74 HCT 123	DIP 16	Dual retriggerable monostable multivibrator with reset	0.61	0.46	0.40
74 HCT 125	DIP 14	Quad buffer/line driver; 3-state			
74 HCT 132	DIP 14	Quad 2-input NAND Schmitt trigger	0.61	0.46	0.40
74 HCT 137	DIP 16	3-to-8 line decoder/demultiplexer with address latches; inverting	1.07	0.80	0.70
74 HCT 138	DIP 16	3-to-8 line decoder/demultiplexer; inverting	0.46	0.35	0.30
74 HCT 139	DIP 16	Dual 2-to-4 line decoder/demultiplexer	0.46	0.35	0.30
74 HCT 153	DIP 16	Dual 4-input multiplexer	0.73	0.55	0.47
74 HCT 154	DIP 24	4-to-16 line decoder/demultiplexer	2.75	2.06	1.79
74 HCT 157	DIP 16	Quad 2-input multiplexer	0.61	0.46	0.40
74 HCT 161	DIP 16	Presetable synchronous 4-bit binary counter; asynchronous reset	0.92	0.69	0.60
74 HCT 162	DIP 16	Presetable synchronous BCD decade counter	1.01	0.76	0.66
74 HCT 163	DIP 16	Presetable synchronous 4-bit binary counter; synchronous reset	0.47	0.35	0.31
74 HCT 164	DIP 14	8-bit serial-in/parallel-out shift register	0.69	0.52	0.45
74 HCT 165	DIP 16	8-bit parallel-in/serial-out shift register	1.16	0.87	0.75
74 HCT 173	DIP 16	Quad D-type flip-flop; positive-edge trigger; 3-state	1.07	0.80	0.70
74 HCT 174	DIP 16	Hex D-type flip-flop with reset; positive-edge trigger	0.92	0.69	0.60
74 HCT 175	DIP 16	Quad D-type flip-flop with reset; positive-edge trigger	0.92	0.69	0.60
74 HCT 193	DIP 16	Presetable synchronous 4-bit binary up/down counter	0.92	0.69	0.60
74 HCT 221	DIP 16	Dual non-retriggerable monostable multivibrator with reset	0.92	0.69	0.60
74 HCT 238	DIP 16	3-to-8 line decoder/demultiplexer	0.98	0.74	0.64
74 HCT 240	DIP 20	Octal buffer/line driver; 3-state; inverting	0.92	0.69	0.60
74 HCT 241	DIP 20	Octal buffer/line driver; 3-state	1.01	0.76	0.66
74 HCT 244	DIP 20	Octal buffer/line driver; 3-state	0.67	0.50	0.44
74 HCT 245	DIP 20	Octal bus transceiver; 3-state	0.67	0.50	0.44

série 74



## CIRCUIT INTEGRE TTL série 74 HCT

CODE	DÉSIGNATION		1	10	25
74 HCT 251	DIP 16	8-input multiplexer; 3-state	0.92	0.69	0.60
74 HCT 257	DIP 16	Quad 2-input multiplexer; 3-state	0.67	0.50	0.44
74 HCT 259	DIP 16	8-bit addressable latch	0.76	0.57	0.49
74 HCT 273	DIP 20	Octal D-type flip-flop with reset; positive-edge trigger	0.67	0.50	0.44
74 HCT 283	DIP 16	4-bit binary full adder with fast carry	1.22	0.92	0.79
74 HCT 299	DIP 20	8-bit universal shift register; 3-state	1.37	1.03	0.89
74 HCT 373	DIP 20	Octal D-type transparent latch; 3-state	0.73	0.55	0.47
74 HCT 374	DIP 20	Octal D-type flip-flop; positive edge-trigger; 3-state	0.73	0.55	0.47
74 HCT 390	DIP 16	Dual decade ripple counter	0.76	0.57	0.49
74 HCT 393	DIP 14	Dual 4-bit binary ripple counter	1.22	0.92	0.79
74 HCT 540	DIP 20	Octal buffer/line driver; 3-state; inverting	0.67	0.50	0.44
74 HCT 541	DIP 20	Octal buffer/line driver; 3-state	0.67	0.50	0.44
74 HCT 573	DIP 20	Octal D-type transparent latch; 3-state	0.67	0.50	0.44
74 HCT 574	DIP 20	Octal D-type flip-flop; positive edge-trigger; 3-state	0.67	0.50	0.44
74 HCT 640	DIP 20	Octal bus transceiver; 3-state; inverting	0.98	0.74	0.64
74 HCT 688	DIP 20	8-bit magnitude comparator	1.22	0.92	0.79
74 HCT 4024	DIP 14	7-stage binary ripple counter	1.04	0.78	0.68
74 HCT 4040	DIP 16	12-stage binary ripple counter	0.73	0.55	0.47
74 HCT 4046	DIP 16	Phase-locked-loop with VCO	1.53	1.15	0.99
74 HCT 4051	DIP 16	8-channel analog multiplexer/demultiplexer	1.83	1.37	1.19
74 HCT 4052	DIP 16	Dual 4-channel analog multiplexer, demultiplexer	1.83	1.37	1.19
74 HCT 4053	DIP 16	Triple 2-channel analog multiplexer/demultiplexer	0.85	0.64	0.55
74 HCT 4060	DIP 16	14-stage binary ripple counter with oscillator	0.73	0.55	0.47
74 HCT 4511	DIP 16	BCD to 7-segment latch/decoder/driver	1.34	1.01	0.87

## CIRCUIT INTEGRE TTL série SN 74 LS

### ■ Spécifications techniques

Alimentation : 5 V. Température d'utilisation : 0° C à + 70° C.

Temps de propagation 9 ns pour une consommation de 2 mW. Boîtier DIP.

CODE	DÉSIGNATION		1	10	25
74 LS 00	DIP 14	Quad 2-input NAND Gate	0.31	0.23	0.20
74 LS 01	DIP 14	Quad 2-Input NAND Gate, Open-Collector	0.31	0.23	0.20
74 LS 02	DIP 14	Quad 2-input NOR Gate	0.37	0.28	0.24
74 LS 03	DIP 14	Quad 2-Input NAND Gate, Open-Collector	0.31	0.23	0.20
74 LS 04	DIP 14	Hex Inverter	0.34	0.26	0.22
74 LS 05	DIP 14	Hex Inverter, Open-Collector	0.31	0.23	0.20
74 LS 08	DIP 14	Quad 2-Input AND Gate	0.31	0.23	0.20
74 LS 09	DIP 14	Quad 2-Input AND Gate, Open Collector	0.40	0.30	0.26
74 LS 10	DIP 14	Triple 3-Input NAND Gate	0.34	0.26	0.22
74 LS 11	DIP 14	Triple 3-Input AND Gate	0.37	0.28	0.24
74 LS 13	DIP 14	Dual 4-Input NAND Schmitt Trigger	0.40	0.30	0.26
74 LS 14	DIP 14	Hex Schmitt-Trigger Inverters	0.40	0.30	0.26
74 LS 15	DIP 14	Triple 3-Input AND Gate, Open-Collector	0.34	0.26	0.22
74 LS 20	DIP 14	Dual 4-input positive-NAND gates	0.40	0.30	0.26
74 LS 21	DIP 14	Dual 4-Input And Gate	0.40	0.30	0.26
74 LS 22	DIP 14	Dual 4-Input NAND Gate, Open Collector	0.43	0.32	0.28
74 LS 24		Integrated Circuit	1.07	0.80	0.70
74 LS 26	DIP 14	Quad 2-Input NAND Buffer, Open Collector	0.34	0.26	0.22
74 LS 27	DIP 14	Triple 3-Input NOR Gate	0.38	0.28	0.25
74 LS 28	DIP 14	Quad 2-Input NOR Buffer	1.00	0.75	0.65
74 LS 30	DIP 14	8-Input NAND Gate	0.43	0.32	0.28
74 LS 32	DIP 14	Quad 2-Input OR Gate	0.34	0.26	0.22
74 LS 33	DIP 14	Quad 2-Input NOR Buffer, Open Collector	0.55	0.41	0.36
74 LS 37	DIP 14	Quad 2-Input NAND Buffer	0.43	0.32	0.28
74 LS 38	DIP 14	Quad 2-Input NAND Buffer, Open Collector	0.43	0.32	0.28
74 LS 42	DIP 16	BCD to Decimal Decoder	0.55	0.44	0.41
74 LS 47	DIP 16	BCD to 7-Segment Decoder/Driver, Open Collector	1.22	0.98	0.92
74 LS 48	DIP 16	BCD to 7-Segment Decoder/Driver	2.25	1.80	1.69



# CIRCUITS INTEGRES

## CIRCUIT INTEGRE TTL

## série SN 74 LS

CODE	DÉSIGNATION		1	10	25
74 LS 51	DIP 14	2 Wide 2/3-Input AND/OR/INVERT Gate	0.46	0.35	0.30
74 LS 54	DIP 14	3-2-2-3-Input AND-OR-INVERT Gate	0.40	0.30	0.26
74 LS 55	DIP 14	2-Wide 4-Input AND-OR-INVERT Gate	0.55	0.41	0.36
74 LS 57	DIP 8	Frequency Dividers	2.14	1.71	1.61
74 LS 73	DIP 14	Dual J-K Flip-Flops with Clear	1.00	0.80	0.75
74 LS 74	DIP 14	Dual D Flip-Flop Positiv-Edge-Triggered Flip-Flops with Preset and Clear	0.34	0.27	0.26
74 LS 75	DIP 16	4-Bit D Latch with Q and NotQ	0.46	0.37	0.35
74 LS 76	DIP 16	Dual J-K Flip-Flops with Preset and Clear	1.37	1.10	1.03
74 LS 85	DIP 16	4-Bit Magnitude Comparator	0.55	0.44	0.41
74 LS 86	DIP 14	Quad 2-Input Exclusive-OR Gates	0.55	0.41	0.36
74 LS 90	DIP 14	Decade Counter	0.61	0.49	0.46
74 LS 91	DIP 14	8-Bit Shift Register	1.37	1.10	1.03
74 LS 92	DIP 14	Divide-by-12 Counter	1.20	0.96	0.90
74 LS 93	DIP 14	4-Bit Binary Counter	1.20	0.96	0.90
74 LS 95	DIP 14	4-Bit Parallel-Access Shift Register			
74 LS 96	DIP 16	5-Bit IN/OUT Shift Register	2.44	1.95	1.83
74 LS 107	DIP 14	Dual J-K Negative Edge-Triggered Flip-Flop with Clear	0.61	0.49	0.46
74 LS 109	DIP 16	Dual J-K Edge-Triggered Flip-Flop with Preset and Clear	0.61	0.49	0.46
74 LS 112	DIP 16	Dual J-K Edge-Triggered Flip-Flop w/Preset			
74 LS 113	DIP 14	DUAL J-K Negative Edge-Triggered Flip-Flop	0.76	0.61	0.57
74 LS 114	DIP 14	DUAL J-K Negative Edge-Triggered Flip-Flop	0.76	0.61	0.57
74 LS 122	DIP 14	Retriggerable Monostable Multivibrators	0.76	0.61	0.57
74 LS 123	DIP 16	Retriggerable Monostable Multivibrators	0.55	0.44	0.41
74 LS 125	DIP 14	Quad 3-State Buffer, Low Enable	0.61	0.46	0.40
74 LS 126	DIP 14	Quad 3-State Buffer, High Enable	0.61	0.46	0.40
74 LS 132	DIP 14	Quad 2-Input NAND Schmitt Trigger	0.61	0.46	0.40
74 LS 136	DIP 14	Quad Exclusive OR Gate, Open-Collector	0.67	0.50	0.44
74 LS 138	DIP 16	1-of-8 Decoder/Demultiplexer	0.55	0.44	0.41
74 LS 139	DIP 16	Dual 1-of-4 Decoder/Demultiplexer	0.61	0.49	0.46
74 LS 145	DIP 16	1-of-10 Decoder/Driver, Open Collector	1.22	0.98	0.92
74 LS 148	DIP 16	8-Input to 3-Line Priority Encoder	0.92	0.74	0.69
74 LS 151	DIP 16	Data Selectors/Multiplexers (8-Input Multiplexer)	0.67	0.54	0.50
74 LS 153	DIP 16	Dual 4-Line To 1-Line Selectors/Multiplexers	0.67	0.54	0.50
74 LS 155	DIP 16	Dual 2-Line To 4-Line Decoders/Demultiplexers	0.61	0.49	0.46
74 LS 156	DIP 16	Dual 2-Line To 4-Line Decoders/Demultiplexers, Open Collector	0.55	0.44	0.41
74 LS 157	DIP 16	Quad 2-Line To 1-Line Selectors/Multiplexers, Non-Inverting	0.70	0.56	0.52
74 LS 158	DIP 16	Quad 2-Line To 1-Line Selectors/Multiplexers, Inverting	0.61	0.49	0.46
74 LS 160	DIP 16	Synchronous Presettable BCD Decade Counter, Asynchronous Master Reset	0.76	0.61	0.57
74 LS 161	DIP 16	Synchronous Presettable 4-Bit Binary Counter, Asynchronous Master Reset	0.61	0.49	0.46
74 LS 162	DIP 16	Synchronous Presettable BCD Decade Counter	0.61	0.49	0.46
74 LS 163	DIP 16	Synchronous Presettable 4-Bit Binary Counter	1.22	0.98	0.92
74 LS 164	DIP 14	8-Bit Serial-in, Parallel-Out Shift Register	0.76	0.61	0.57
74 LS 165	DIP 16	8-Bit Parallel-To-Serial Shift Register	1.07	0.86	0.80
74 LS 166	DIP 16	8-Bit Shift Register	0.70	0.56	0.52
74 LS 168	DIP 16	Up/Down BCD Decade Counter	1.22	0.98	0.92
74 LS 169	DIP 16	Module 16 Binary Up/Down Counter	0.76	0.61	0.57
74 LS 170	DIP 16	4x4 Register File, Open-Collector	1.83	1.46	1.37
74 LS 173	DIP 16	4-Bit D-Type Register, 3_State Outputs	0.76	0.61	0.57
74 LS 174	DIP 16	Hex D-Type Flip-Flop, Master Reset	0.64	0.51	0.48
74 LS 175	DIP 16	Quad D-Type Flip-Flop with Clear	0.76	0.61	0.57
74 LS 181	DIP 24	4-Bit Arithmetic Logic Unit	1.83	1.46	1.37
74 LS 191	DIP 16	Synchronous Up/Down Binary Counters with Down/Up Mode Control	0.92	0.74	0.69
74 LS 193	DIP 16	Presettable Binary Up/Down Counter	0.76	0.61	0.57
74 LS 195	DIP 16	4-Bit Parallel Access Shift Register (9300 Type)	1.22	0.98	0.92
74 LS 196	DIP 14	Presettable Decade Counters/Latches	0.76	0.61	0.57
74 LS 197	DIP 14	Presettable 4-Bit Binary Counters/Latches	1.22	0.98	0.92
74 LS 221	DIP 16	Dual Monostable Multivibrator with Schnitt-Trigger Inputs	0.92	0.74	0.69

série 74



## CIRCUIT INTEGRE TTL

série SN 74 LS

CODE	DÉSIGNATION	1	10	25
74 LS 240	DIP 20 Octal Buffer/Line Driver/3-State, Inverting	0.92	0.74	0.69
74 LS 241	DIP 20 Octal Buffer/Line Driver/3-State, Non-Inverting	0.92	0.74	0.69
74 LS 243	DIP 14 Quad Bus Transceiver, Non-Inverting	0.92	0.74	0.69
74 LS 244	DIP 20 Octal Buffer/Line Driver/3-State, Non-Inverting	0.92	0.74	0.69
74 LS 245	DIP 14 Octal Bidirectional Transceiver/3-State, Non-Inverting	0.61	0.49	0.46
74 LS 247	DIP 16 BCD to 7-Segment Decoder/Driver, Open Collector	0.76	0.61	0.57
74 LS 251	DIP 16 8-Input Multiplexer, 3-State	0.76	0.61	0.57
74 LS 253	DIP 16 Dual 4-Input Multiplexer, 3-State	0.76	0.61	0.57
74 LS 257	DIP 16 Quad 2-Input Multiplexer, Non-Inverting 3-State	0.76	0.61	0.57
74 LS 258	DIP 16 Quad 2-Input Multiplexer, Inverting 3-State	0.76	0.61	0.57
74 LS 259	DIP 16 8-Bit Addressable Latch (9334)	0.92	0.74	0.69
74 LS 261	DIP 16 Programmable Binary Multiplexer	1.83	1.46	1.37
74 LS 266	DIP 14 Quad Exclusive NOR Gate, Open-Collector	0.61	0.46	0.40
74 LS 273	DIP 20 Octal D-Type Flip-Flop with Clear	0.76	0.61	0.57
74 LS 279	DIP 16 Quad Set-Reset Latches	0.76	0.61	0.57
74 LS 280	DIP 14 9-Bit Odd/Even Parity Generator/Checker	0.76	0.61	0.57
74 LS 283	DIP 16 4-Bit Full Adder (Rotated LS83A)	0.70	0.56	0.52
74 LS 290	DIP 14 Decade Counter	0.76	0.61	0.57
74 LS 293	DIP 14 4-Bit Binary Counter	0.76	0.61	0.57
74 LS 299	DIP 20 8-Bit Universal Shift/Storage Register with Common Parallel I/O Pins, 30-State	1.83	1.46	1.37
74 LS 323	DIP 20 8-Input Shift/Storage Register with Synchronous Reset and Common I/O Pins, 3-State	2.75	2.20	2.06
74 LS 353	DIP 16 Dual 4-Input Multiplexer/3-State LS352	0.92	0.74	0.69
74 LS 365	DIP 16 Hex Buffer with Common Enable, Non-Inverting, 3-State	0.67	0.50	0.44
74 LS 366	DIP 16 Hex Inverting Buffer with Common Enable, 3-State	0.76	0.57	0.49
74 LS 367	DIP 16 Hex Buffer, 2/4 Bit, Non-Inverting, 3-State	0.61	0.46	0.40
74 LS 373	DIP 20 Octal Transparent Latch/3-State	0.92	0.74	0.69
74 LS 374	DIP 20 Octal D-Type Flip-Flop/3-State	0.92	0.74	0.69
74 LS 375	DIP 16 4-Bit D-Type Latch with Q and NotQ	0.92	0.74	0.69
74 LS 377	DIP 20 Octal D-Type Flip-Flop with Enable	0.92	0.74	0.69
74 LS 378	DIP 16 Parallel Hex D-Type Register, with Enable	1.22	0.98	0.92
74 LS 379	DIP 16 Quad Parallel Register, with Enable	1.22	0.98	0.92
74 LS 390	DIP 16 Dual Decade Counter	0.70	0.56	0.52
74 LS 395	DIP 16 4-Bit Shift Register, 3-State			
74 LS 393	DIP 14 Dual 4-Bit Binary Counter	0.92	0.74	0.69
74 LS 465	DIP 20 Octal Buffers With 3-State Outputs	1.37	1.10	1.03
74 LS 490	DIP 16 Dual Decade Counter	0.76	0.61	0.57
74 LS 541	DIP 20 Octal 3-State Driver, Non-Inverting	1.22	0.98	0.92
74 LS 573	DIP 20 Octal D-Type Latch	1.22	0.98	0.92
74 LS 640	DIP 20 Octal Bus Transceiver Inverting with 3-State Outputs	1.22	0.98	0.92
74 LS 641	DIP 20 Octal Bus Transceiver, Open Collector	1.80	1.44	1.35
74 LS 645	DIP 20 Octal Bus Transceiver	1.22	0.98	0.92
74 LS 645 1	DIP 20 Octal Bus Transceiver/IOL=48 mA 3-State	1.49	1.19	1.12
74 LS 670	DIP 16 4x4 Register File, 3-State	0.92	0.74	0.69
74 LS 682	DIP 20 8-Bit Magnitude Comparator	2.44	1.95	1.83
74 LS 684	DIP 20 8-Bit Magnitude Comparator	2.59	2.07	1.94
74 LS 688	DIP 20 8-Bit Magnitude Comparator	1.83	1.46	1.37

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# CIRCUITS INTEGRES

CIRCUIT INTEGRE TTL

série SN 74

CODE	DÉSIGNATION	1	10	25
74 01	DIP 14 Quad 2-input open-collector NAND gates	0.92	0.74	0.69
74 03	DIP 14 Quad 2-input open-collector NAND gates	0.92	0.74	0.69
74 04	DIP 14 Hex inverters	0.92	0.74	0.69
74 05	DIP 14 Hex inverters with open collector outputs	0.92	0.74	0.69
74 06	DIP 14 Hex inverter buffers / drivers with high-voltage outputs	1.01	0.81	0.76
74 07	DIP 14 Hex Buffers/Drivers with Open-Collector High-Voltage Outputs	0.92	0.74	0.69
74 10	DIP 14 Triple 3-Input NAND Gate	1.07	0.86	0.80
74 12	DIP 14 Triple 3-Input NAND Gate, Open Collector	1.07	0.86	0.80
74 16	DIP 14 Hex Inverter Buffers/Drivers with Open-Collector High-Voltage Outputs	0.92	0.74	0.69
74 17	DIP 14 Hex Buffers/Drivers with Open-Collector High-Voltage Outputs	0.99	0.79	0.74
74 20	DIP 14 Dual 4-Input Nand Gate	1.07	0.86	0.80
74 23	DIP 14 Dual 4-Input NOR Gates with Strobe	1.07	0.86	0.80
74 25	DIP 14 Dual 4-Input NOR Gates with Strobe	0.92	0.74	0.69
74 26	DIP 14 Quad 2-Input NAND Buffer, Open Collector	1.07	0.86	0.80
74 32	DIP 14 Quad 2-Input OR Gate	1.30	1.04	0.97
74 38	DIP 14 Quad 2-Input NAND Buffer, Open Collector	1.07	0.86	0.80
74 40	DIP 14 Dual 4-Input NAND Buffer	0.92	0.74	0.69
74 42	DIP 16 BCD Decimal Decoder	1.83	1.46	1.37
74 43	DIP 16 Ex 3 To Decimal Decoder	1.83	1.46	1.37
74 44	DIP 16 4 to 10 Line Decoder	1.83	1.46	1.37
74 45	DIP 16 BCD-To-Decimal Decoders/Drivers	2.75	2.20	2.06
74 46	DIP 16 BCD to 7-Segment Decoder/Driver	2.75	2.20	2.06
74 47	DIP 16 BCD to 7-Segment Decoder/Driver, Open Collector	2.75	2.20	2.06
74 54	DIP 14 3-2-2-3-Input AND-OR-INVERT Gate	0.76	0.61	0.57
74 60	DIP 14 Dual 4 Input Expander	1.07	0.86	0.80
74 74	DIP 14 Dual D Flip-Flop Positiv-Edge-Triggered Flip-Flops with Preset and Clear	0.92	0.74	0.69
74 75	DIP 16 4-Bit D Latch with Q and NotQ	1.37	1.10	1.03
74 81	DIP 14 16 Bit RAM	2.75	2.20	2.06
74 91	DIP 14 8-Bit Shift Register	1.22	0.98	0.92
74 92	DIP 14 Divide-by-12 Counter	1.37	1.10	1.03
74 97	DIP 16 Synchronous 6-Bit Binary Rate Multipliers	2.75	2.20	2.06
74 104	DIP 14 J-K M/S FLIP FLOP	0.88	0.70	0.66
74 107	DIP 14 Dual J-K Negative Edge-Triggered Flip-Flop with Clear	1.22	0.98	0.92
74 109	DIP 16 Dual J-K Edge-Triggered Flip-Flop with Preset and Clear	0.92	0.74	0.69
74 116	DIP 24 Dual 4-Bit Latches with Clear	3.35	2.68	2.51
74 118	DIP 16 4 RS-Flip Flop	2.13	1.70	1.60
74 120	DIP 16 Dual Pulse Synchronizers/Drivers	2.75	2.20	2.06
74 121	DIP 14 Monostable Multivibrator with Schmitt-Trigger inputs	1.53	1.22	1.15
74 128	DIP 14 Line Drivers	1.37	1.10	1.03
74 132	DIP 14 Quad 2-Input NAND Schmitt Trigger	1.37	1.10	1.03
74 142	DIP 16 BCD Control Latch Driver	4.27	3.42	3.20
74 144	DIP 24 4-Bit Control Latch Driver	6.40	5.12	4.80
74 150	DIP 24 Data Selectors/Multiplexers	2.75	2.20	2.06
74 151	DIP 16 Data Selectors/Multiplexers (8-Input Multiplexer)	1.22	0.98	0.92
74 153	DIP 16 Dual 4-Line To 1-Line Selectors/Multiplexers	1.22	0.98	0.92
74 154	DIP 24 4-Line To 16-Line Decoders/Demultiplexers	2.75	2.20	2.06
74 155	DIP 16 Dual 2-Line To 4-Line Decoders/Demultiplexers	0.92	0.74	0.69
74 157	DIP 16 Quad 2-Line To 1-Line Selectors/Multiplexers, Non-Inverting	1.37	1.10	1.03
74 160	DIP 16 Synchronous Presettable BCD Decade Counter, Asynchronous Master Reset	1.78	1.42	1.33
74 161	DIP 16 Synchronous Presettable 4-Bit Binary Counter, Asynchronous Master Reset	1.83	1.46	1.37
74 162	DIP 16 Synchronous Presettable BCD Decade Counter	2.14	1.71	1.61
74 165	DIP 16 8-Bit Parallel-To-Serial Shift Register	2.14	1.71	1.61
74 170	DIP 16 4x4 Register File, Open-Collector	1.83	1.46	1.37
74 172	DIP 24 16-Bit Multiple-Port Register File with 3-State Outputs	5.49	4.39	4.12
74 176	DIP 14 35-MHz Presettable Decade and Binary Counters/Latches	1.53	1.22	1.15
74 179	DIP 16 4-Bit Shift Register DC	1.22	0.98	0.92

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## CIRCUIT INTEGRE TTL série SN 74

CODE	DÉSIGNATION		1	10	25
74 180	DIP 14	9-Bit Odd/Even Parity Generators/Checkers	2.14	1.71	1.61
74 182	DIP 16	Look Ahead Carry Generator	2.44	1.95	1.83
74 184	DIP 16	BCD to Binary Converter	2.14	1.71	1.61
74 191	DIP 16	Synchronous Up/Down Binary Counters with Down/Up Mode Control	0.92	0.74	0.69
74 193	DIP 16	Presetable Binary Up/Down Counter	3.35	2.68	2.51
74 196	DIP 14	Presetable Decade Counters/Latches	2.14	1.71	1.61
74 199	DIP 24	8-Bit Shift Register			
74 221	DIP 16	Dual Monostable Multivibrator with Schmitt-Trigger Inputs	1.83	1.46	1.37
74 247	DIP 8	BCD to 7-Segment Decoder/Driver, Open Collector	3.66	2.93	2.75
74 259	DIP 16	8-Bit Addressable Latch	3.75	3.00	2.81
74 279	DIP 16	Quad Set-Reset Latches	3.25	2.60	2.44
74 283	DIP 16	4-Bit Full Adder	2.42	1.94	1.82
74 285	DIP 16	4-Bit by 4-Bit Parallel Binary Multipliers	3.35	2.68	2.51
74 390	DIP 16	Dual Decade Counter	2.14	1.71	1.61
74 393	DIP 14	Dual 4-Bit Binary Counter	3.35	1.71	1.61

## CIRCUIT INTEGRE TTL série 74 ACT

CODE	DÉSIGNATION		1	10	25
74 AC 08	DIP 14	Quad 2-Input AND Gate	0.73	0.73	0.73
74 ACT 04	DIP 14	Hex Inverter	0.67	0.54	0.50
74 ACT 05	DIP 14	Hex inverter, open drain outputs	0.75	0.60	0.56
74 ACT 14	DIP 14	Hex Inverter Schmitt Trigger Input	0.92	0.74	0.69
74 ACT 74	DIP 14	Dual D-Type Positive Edge-Triggered Flip-Flop	1.07	0.86	0.80
74 ACT 245	DIP 20	Octal Bidirectional Transceiver with 3-STATE Inputs/ Outputs	1.53	1.22	1.15
74 ACT 323	DIP 20	8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins	1.22	0.98	0.92

## CIRCUIT INTEGRE TTL série DM 74 ALS

CODE	DÉSIGNATION		1	10	25
74 ALS 00	DIP 14	Quad 2-Input NAND Gates	0.61	0.49	0.46
74 ALS 04	DIP 14	Hex Inverters	0.36	0.29	0.27
74 ALS 08	DIP 14	Quad 2-Input AND Gate	0.61	0.49	0.46
74 ALS 10	DIP 14	Triple 3-Input NAND Gates	0.67	0.54	0.50
74 ALS 20	DIP 14	Dual 4-Input NAND Gates	0.61	0.49	0.46
74 ALS 21	DIP 14	Dual 4-Input AND Gates	0.61	0.49	0.46
74 ALS 27	DIP 14	Triple 3-Input NOR Gates	0.61	0.49	0.46
74 ALS 32	DIP 14	Quad 2-Input OR Gate	0.61	0.49	0.46
74 ALS 133	DIP 16	13-Input NAND Gate	0.73	0.58	0.55
74 ALS 138	DIP 16	3 to 8 Line Decoder/Demultiplexer	1.07	0.86	0.80
74 ALS 139	DIP 16	Dual 1-of-4 decoder/demultiplexer	1.07	0.86	0.80
74 ALS 257	DIP 16	3-STATE Quad 1-of-2 Line Data Selector/Multiplexer	1.22	0.98	0.92
74 ALS 373	DIP 20	Octal D-Type 3-STATE Transparent Latches	1.53	1.22	1.15
74 ALS 541	DIP 20	Octal Buffers and Line Drivers with 3-STATE Outputs	1.66	1.33	1.24
74 ALS 574	DIP 20	Octal D-Type Edge Triggered Flip-Flops with 3-STATE Outputs	1.37	1.10	1.03
74 ALS 576	DIP 20	Octal D-Type Edge-Triggered Flip-Flops with 3-STATE Outputs	1.83	1.46	1.37
74 ALS 641ADW	DIP 20	Octal Bus Transceivers With Open-Collector Outputs	2.44	1.95	1.83
74 ALS 645	DIP 20	Octal Bus Transceivers	2.14	1.71	1.61
74 ALS 688	DIP 20	8-Bit Identity Comparators	5.49	4.39	4.12

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# CIRCUITS INTEGRES

## CIRCUIT INTEGRE TTL

série DM 74 AS

CODE	DÉSIGNATION		1	10	25
74 AS 04	DIP 14	Hex Inverter	1.24	1.24	1.24
74 AS 373	DIP 20	Octal D-Type Transparent Latch with 3-STATE Outputs	3.96	3.96	3.96

## CIRCUIT INTEGRE TTL

série 74 F

CODE	DÉSIGNATION		1	10	25
74 F 00	DIP 14	Quad 2-Input NAND Gate	0.61	0.49	0.46
74 F 02	DIP 14	Quad 2-Input NOR Gate	0.64	0.51	0.48
74 F 08	DIP 14	Quad 2-Input AND Gate	0.76	0.61	0.57
74 F 20	DIP 14	Dual 4-Input NAND Gate	0.92	0.74	0.69
74 F 74	DIP 14	Dual D-Type Positive Edge-Triggered Flip-Flop	0.76	0.61	0.57
74 F 125	DIP 14	3-state Quad Buffer	1.07	0.86	0.80
74 F 126	DIP 14	3-state Quad Buffer	1.07	0.86	0.80
74 F 161	DIP 16	Synchronous Presettable 4-Bit Binary Counter (Asynchronous Reset)	1.37	1.10	1.03
74 F 194	DIP 16	4-Bit Bidirectional Universal Shift Register	2.14	1.71	1.61
74 F 244	DIP 20	Octal Buffer/Line Driver with 3-STATE Outputs	0.92	0.74	0.69
74 F 245	DIP 20	Octal Bidirectional Transceiver with 3-STATE Inputs/Outputs	0.92	0.74	0.69
74 F 269	DIP 24	8-Bit Bidirectional Binary Counter	3.93	3.14	2.95
74 F 521	DIP 20	8-Bit Identity Comparator	0.92	0.74	0.69
74 F 534	DIP 20	Octal D-Type Flip-Flop with 3-STATE Outputs	1.22	0.98	0.92

## CIRCUIT INTEGRE TTL

série 74 C

CODE	DÉSIGNATION		1	10	25
74 C 00	DIP 14	Quad 2-Input NAND Gate	0.79	0.63	0.59
74 C 02	DIP 14	Quad 2-Input NOR Gate	0.79	0.63	0.59
74 C 04	DIP 14	Hex Inverter	0.46	0.37	0.35
74 C 08	DIP 14	Quad 2-Input AND Gate	0.46	0.37	0.35
74 C 10	DIP 14	Triple 3-Input NAND Gates	0.79	0.63	0.59
74 C 20	DIP 14	Dual 4-Input NAND Gate	0.92	0.74	0.69
74 C 30	DIP 14	8-Input NAND Gate	0.79	0.63	0.59
74 C 42	DIP 16	BCD-to-Decimal Decoder	1.37	1.10	1.03
74 C 48	DIP 16	BCD-to-7 Segment Decoder	3.05	2.44	2.29
74 C 73	DIP 14	Dual J-K Flip-Flops with Clear and Preset	1.37	1.10	1.03
74 C 74	DIP 14	Dual D-Type Flip-Flop	2.40	1.92	1.80
74 C 76	DIP 16	Dual J-K Flip-Flops with Clear and Preset	1.37	1.10	1.03
74 C 83	DIP 16	4-Bit Binary Full Adder	4.93	3.94	3.70
74 C 85	DIP 16	4-Bit Magnitude Comparator	1.87	1.50	1.40
74 C 89	DIP 16	64-Bit 3-STATE Random Access Read/Write Memory	12.50	10.00	9.38
74 C 90	DIP 14	4-Bit Decade Counter	1.83	1.46	1.37
74 C 93	DIP 14	4-Bit Binary Counter	2.75	2.20	2.06
74 C 150	DIP 24	16 to 1 line decoder	11.59	9.27	8.69
74 C 154	DIP 24	4-Line to 16-Line Decoder/Demultiplexer	8.10	6.48	6.08
74 C 164	DIP 14	8-Bit Parallel-Out Serial Shift Register	1.37	1.10	1.03
74 C 192	DIP 16	Synchronous BCD Up/Down Dual Clock Counter	1.83	1.46	1.37
74 C 193	DIP 16	Synchronous Binary Up/Down Dual Clock Counter	0.92	0.74	0.69
74 C 221	DIP 16	Dual Monostable Multivibrator	2.29	1.83	1.72
74 C 240	DIP 20	Inverting Octal Buffer and Line Driver with 3-STATE Outputs	5.92	4.74	4.44

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## CIRCUIT INTEGRE TTL

série 74 C

CODE	DÉSIGNATION		1	10	25
74 C 902	DIP 14	Hex Non-Inverting TTL Buffer	1.37	1.10	1.03
74 C 906	DIP 14	Hex Open Drain N-Channel Buffers	1.37	1.10	1.03
74 C 908	DIP 8	Dual CMOS 30-Volt Relay Driver	3.93	3.14	2.95
74 C 909	DIP 14	Quad* comparator	2.75	2.20	2.06
74 C 914	DIP 14	Hex Schmitt Trigger with Extended Input Voltage	4.27	3.42	3.20
74 C 922	DIP 18	CMOS 16 Key Keyboard Encoder	6.40	5.12	4.80
74 C 923	DIP 20	CMOS 20 Key Keyboard Encoder	7.93	6.34	5.95
74 C 925	DIP 16	CMOS 4 Digit Counter	12.35	9.88	9.26
74 C 926	DIP 18	CMOS 4-Digit Counter With Carry	18.75	15.00	14.06
74 C 927	DIP 18	4-Digit Multiplexed Output	18.75	15.00	14.06
74 C 928	DIP 18	4 Digit Counter W/ Segment DRV	18.75	15.00	14.06

## CIRCUIT INTEGRE TTL

série SN 74 S

CODE	DÉSIGNATION		1	10	25
74 S 37	DIP 14	Quad 2-input positive-NAND buffers	1.37	1.10	1.03
74 S 74	DIP 14	Dual D-Type Positive-Edge-Triggered Flip-Flops With Preset And Clear	1.22	0.98	0.92
74 S 86	DIP 14	Quad 2-input Exclusive-OR gates	1.22	0.98	0.92
74 S 124	DIP 16	Dual voltage-controlled oscillators	3.96	3.17	2.97
74 S 133	DIP 16	13-Input Positive-NAND Gates	0.92	0.74	0.69
74 S 134	DIP 16	12 Input NAND Gate 3 State	1.37	1.10	1.03
74 S 138	DIP 16	3-line to 8-line decoder / demultiplexer	1.37	1.10	1.03
74 S 140	DIP 14	Dual 4-input positive-NAND 50-Ohm line drivers	1.37	1.10	1.03
74 S 163	DIP 16	4-Bit Binary Counters	2.29	1.83	1.72
74 S 174	DIP 16	Hex D-Type Flip-Flops With Clear	0.76	0.61	0.57
74 S 189	DIP 16	16X4-Bit RAM	1.71	1.71	1.61
74 S 226	DIP 16	Circuit intégré	3.96	3.17	2.97
74 S 374	DIP 20	Octal D-Type Positive Edge Triggered Flip-Flops with 3-State Outputs	2.53	2.02	1.90

## CIRCUIT INTEGRE TTL

série SN 75

CODE	DÉSIGNATION		1	10	25
75 107	DIP 14	Dual Line Receiver	1.46	1.31	1.24
75 112	DIP 14	Dual Line Driver	4.27	3.84	3.63
75 114	DIP 16	Dual Differential Line Driver	2.29	2.06	1.95
75 115	DIP 16	Dual Differential Line Receiver	1.92	1.73	1.63
75 121	DIP 16	Dual Line Drivers	2.32	2.09	1.97
75 122	DIP 16	Triple Line Receivers	1.92	1.73	1.63
75 140	DIP 8	Dual Line Receiver	2.88	2.59	2.45
75 150	DIP 8	Dual Line Driver	1.32	1.19	1.12
75 154	DIP 16	Quadruple Differential Line Receiver	2.33	2.10	1.98
75 160	DIP 20	Octal General-Purpose Interface Bus Transceiver	3.35	3.01	2.85
75 161	DIP 20	Octal General-Purpose Interface Bus Transceiver	5.03	4.53	4.28
75 162	DIP 22	Octal General-Purpose Interface Bus Transceiver	5.18	4.66	4.40
75 163	DIP 20	Circuit intégré	10.31	9.28	8.76
75 369	DIP 14	Interface Dual Mos Clock driver	4.35	3.91	3.70
75 451	DIP 8	Dual Very-High Speed, High-Current Peripheral Drivers /AND	1.05	0.94	0.89
75 453	DIP 8	Dual Very-High Speed, High-Current Peripheral Drivers /OR	1.10	0.99	0.94
75 454	DIP 8	Dual Very-High Speed, High-Current Peripheral Drivers /NOR	1.10	0.99	0.94
75 462P	DIP 8	Dual High-Voltage, High-Current Peripheral Drivers	1.52	1.37	1.29
75 469	DIP 16	High-Voltage, High-Current Darlington Transistor Arrays	3.05	2.74	2.59
75 471	DIP 8	Dual High-Voltage, High-Current Peripheral Drivers /AND	1.86	1.67	1.58
75 472	DIP 8	Dual High-Voltage, High-Current Peripheral Drivers /NAND	1.35	1.22	1.15

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